Fabrication and Characterization of ZnO based Thin Film Transistors with HfO_2 as Dielectric Material

A DISSERTATION SUBMITTED IN PARTIAL FULFILLMENT
FOR THE REQUIREMENTS OF THE DEGREE OF

Integrated Master of Science
IN
Physics

BY

Agnish Dev Prusty
(410ph5027)

UNDER THE GUIDANCE OF

Dr. Jyoti Prakash Kar

Department of Physics & Astronomy

NATIONAL INSTITUTE OF TECHNOLOGY

Rourkela - 769008,
Odisha, India.
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Abstract

HfO_2 thin films were prepared using reactive RF magnetron sputtering of a pure hafnium target in argon and oxygen ambient onto heavily doped p^{++} silicon (100) substrates. ZnO semiconducting thin film channel was deposited using sputtering of a pure metallic zinc target in oxygen ambient over the already deposited dielectric layer and the metallization for contact electrodes was done using thermal evaporation system. The thin film transistors (TFTs) were also fabricated with copper and aluminum as gate material other than heavily doped silicon. Besides TFT, metal-insulator-metal (MIM) and metal-oxide-semiconductor (MOS) structures were also made using HfO_2 as oxide dielectric layer. The dielectric layer thickness, along with various growth parameters were studied and optimized using the various electrical characterization results from MOS, MIM and FET devices, to know the limit of oxide thickness that can provide sufficient charge polarization and electric field for channel conduction at lower gate voltages while giving low leakage current for the successful operation of the field-effect transistor (FET) device.

CERTIFICATE

Department of Physics & Astronomy
National institute of Technology
Rourkela - 769008, Odisha, India.

This is to certify that the project work in the thesis entitled, **"Fabrication and Characterization of ZnO based Thin Film Transistors with HfO_2 as** Dielectric Material**"** represents the authentic research work carried out byAgnish Dev Prusty, in partial fulfillment for the degree of Integrated Master of Science in Physics at National Institute of Technology Rourkela, under my supervision. The work is satisfactory to the best of my knowledge.

Dr.Jyoti Prakash Kar
Assistant Professor
Department of Physics & Astronomy
NIT Rourkela-769008
Odisha, India

Date: 11^{th} May, 2015
Place: Rourkela

DECLARATION

I, the undersigned *Mr.Agnish Dev Prusty*, hereby declare that the work reported in the masters thesis entitled, **"Fabrication and Characterization of ZnO based Thin Film Transistors with HfO_2 as Dielectric Material"**, submitted in partial fulfilment for the degree of Integrated Master of Science, is a result of authentic research carried out between July 2013 and May 2015 at National Institute of Technology, Rourkela. Work by other investigators referenced in the text is highly acknowledged.

Agnish Dev Prusty
Date: **11^{th} May, 2015**

Dedicated to my family

Acknowledgment

I take this opportunity to express my profound gratitude and deep regards from the core of my heart to my research supervisor *Dr.Jyoti Prakash Kar* for his exemplary guidance, monitoring and constant encouragement throughout the course of the masters project. The blessings, help, motivation, lessons and guidance given by him from time to time shall carry me a long way in the journey of life on which I am about to embark.

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Lastly, I thank the ubiquitous creator of the beautiful creation, my parents, special relatives and friends for their perennial encouragement.

Agnish Dev Prusty

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Outline

Staggered bottom-gate thin film transistors (TFTs) were fabricated with three different gate substrates such as heavily doped p^{++} silicon (100), copper and glass-aluminum. The hafnium oxide thin film was deposited over these substrates using reactive RF magnetron sputtering system. Then, zinc oxide thin film semiconducting channel was also deposited using sputtering system and finally the source-drain electrodes using characteristic mask in a thermal evaporation system. Pure grade aluminum has been used everywhere for metallization. Other than these FETs, MIM and MOS structures were also fabricated with hafnium oxide as the high-k dielectric layer. For MIM device, the zinc oxide film is absent and the rest layers are same. For MOS device, the semiconducting substrate is p-type (100) silicon, the ZnO layer is absent and the rest layers are same. In case of glass-aluminum as gate, aluminum layer was deposited globally over the cleaned glass substrate. For MIM and MOS structure, aluminum as top-side terminals was deposited locally using the same mask but for FET device, the source-drain terminals were deposited locally using a special characteristic feature mask. In case of MOS device, the bottom side of the silicon substrate was given a global aluminum layer for other end contact terminal.

The thin film thickness measurement, X-ray diffraction and UV-Visible spectroscopy was done for the dielectric and semiconducting thin films. The I-V (current-voltage) and C-V (capacitance-voltage) characteristics of MOS and MIM structures were studied. The output and transfer characteristics were examined for the FET device and the leakage current was observed for the thin film transistor. All these electrical characterization results on devices with three different gate materials are utilized to manipulate the fabrication conditions of dielectric layer to find the optimized limiting conditions.

The thesis entitled, "Fabrication and Characterization of ZnO based Thin Film Transistors with HfO_2 as High-k Dielectric Layer" contains four chapters in total. The following are the piecewise description about a brief overview of each of the chapters.

Chapter 1 outlines the initial developments from vacuum tubes, vacuum diodes, triodes to transistor. It explains the basic concept of thin film transistor and the need of high-k dielectric materials while touching through the basic concept of equivalent oxide thickness. It also elucidates the reason for choosing of hafnium oxide and zinc oxide along with their material properties.

Chapter 2 makes you visualize all the schematic diagrams, i.e. device layout of various devices fabricated such as MOS, MIM and FET. A brief description about the fabrication technologies utilized are specified, followed by the experimental work done that was done in the whole span of fabrication with various process parameters.

Chapter 3 gives an insight into the various structural, optical and electrical characterization techniques that were carried out with the thin films along with images of those instruments that are present in our laboratory and the ones that were used from other sources. It also touches some of the modes in measuring the thickness of a thin film.

Chapter 4 discusses about the various results obtained from the different characterization techniques to interpret useful information and separate out the unwanted results that is not worth for further investigation.

All these chapters are finally followed by a brief conclusion, scope for future work and references provided in the text.

Chapter 1

Introduction

In recent decades, the world of computing has seen wonders in terms of processing speeds. This is all due to the rapid advancements in technology associated with the microelectronics industry. The miniaturization and scaling down of semiconductor electronic devices has got varied applications in different sectors. It is used in smart sensors, flat panel TFT displays, microprocessor circuits in computing systems, etc. This whole thesis revolves around the use and optimization of high-k dielectric that has helped reduce this problem up to some extent, since, it again has got its own merits as well as limitations.

1.1 History of Triodes to Transistor

Initially, devices that needed to amplify a signal such as in radios or early computers used the vacuum-tube amplifier. This was the triode which was a glass tube containing a heater filament, a heated emitter plate (cathode) that emits electrons and a collector plate (anode) that collects the electrons once they have been accelerated through the tube with a metal grid in between. Since the device had three active elements namely the anode, the cathode, and the grid, hence, the name triode. Small changes to the grid voltage can cause large changes in the electron current flowing to the collector plate. If the grid is removed, then the device becomes simply a vacuum-tube diode. Vacuum tube triodes, also known as thermionic valves worked for many purposes but they were bulky, slowly operating and consumed high power. So, for quite a long time, researchers across the globe attempted to make a solid-state version of the device with an attempt to allow creation of a smaller, faster and less power-hungry electronic device. The field-effect transistor was patented by the German scientist Julius Lilienfeld in 1926 but it never worked properly. Meanwhile, in 1938, the German physicist Robert Pohl made a solid-state amplifier using a salt as the semiconductor. This device worked but reacted to signals too slowly to be of any use. Ultimately, three scientists John Bardeen, Walter Brattain, and William Shockley working at Bell Laboratories discovered the first workable solid-state transistor on December 23, 1947 for which they got the Nobel Prize.

A month later after the development of the point-contact transistor, Shockley realized that Russell Ohl's p-type and n-type semiconductors in combination made it possible to build a solid-state analog of the vacuum tube triode. So, the solution was to sandwich a thin p-type semiconductor in between two n-type pieces, resulting in two p-n junctions (two diodes) operating front to front. A current applied to the p-type layer could control the current between the two n-type regions. This resulting bipolar transistor proved much more reliable than the point-contact transistor. In the bipolar transistor as in the then modern transistors, the essential junctions between the p-type and n-type layers were buried deep within the semiconductor crystal where they cannot be affected by their ambient.

There are two types of transistors in use today, the bipolar transistor, often called the bipolar junction transistor (BJT) and the field-effect transistor (FET). The BJT is composed of two closely coupled p-n junctions, and is bipolar for the fact that both electrons and holes are involved in the conduction process. BJT is a current controlled device that has base, emitter and collector electrodes which is able to deliver a change in output voltage in response to a change in input current with a low input impedance. It is widely used as an amplifier and is a key component in oscillators, high-speed

integrated circuits, and switching circuits. But the FET is a unipolar device, as its conducting pathway involves only one kind of charge carrier. It can be built either as a metal-oxide-semiconductor field-effect transistor (MOSFET) or as a junction field-effect transistor (JFET). FET is a voltage controlled device with a high input impedance that has gate, source, and drain electrodes.

1.2 Thin Film Transistor

A transistor is a three terminal active semiconductor device used for amplifying and switching of electronic signals and electrical power. The three terminals are used for connection to an external circuit and the basic mechanism is that current in a pair of terminals is modulated and controlled by the voltage in the third terminal.

A thin film transistor is a special kind of field-effect transistor made by depositing thin films of an active semiconductor layer as well as the dielectric layer and metallic contacts over a supporting substrate. Compared to bulk transistors, thin film transistors have the advantageous fact that they have a large effective surface area for both the semiconducting and dielectric thin films. This gives the added advantage for modulating the properties at the interface and hence the overall properties of the transistor. This property allows the transistor to act as a good sensor and also have higher switching speeds for microprocessor circuits and small feature size makes it suitable for VLSI and embedded systems. The ability of reducing the thickness of films makes it a suitable candidate where scaling down is required. Another advantage is that one can build stack layers of different dielectric material with varied properties for a single transistor. These capacitances in series will give different dielectric properties to the device and one can play with the amorphous nature of various layers to reduce the leakage current.

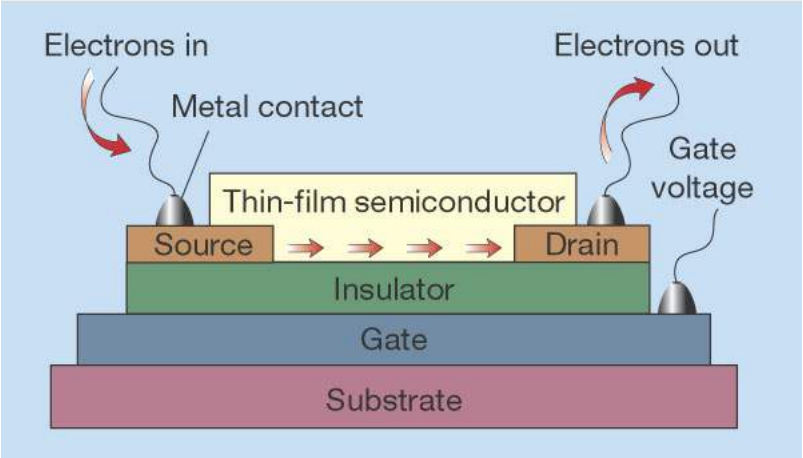

Figure 1.1: Basic schematic of a thin film transistor

There are two types of TFT based on the position of gate material:
1. Top - gate TFT
2. Bottom - gate TFT

There are two types of TFT based on the position of source-drain electrodes and semiconducting thin film layer:
1. Staggered TFT
2. Coplanar TFT

So, there are four possible combinations for a TFT construction such as:
1. Top-gate staggered TFT
2. Top-gate coplanar TFT
3. Bottom-gate staggered TFT
4. Bottom-gate coplanar TFT

All the FETs reported in this thesis are staggered bottom gate TFTs.

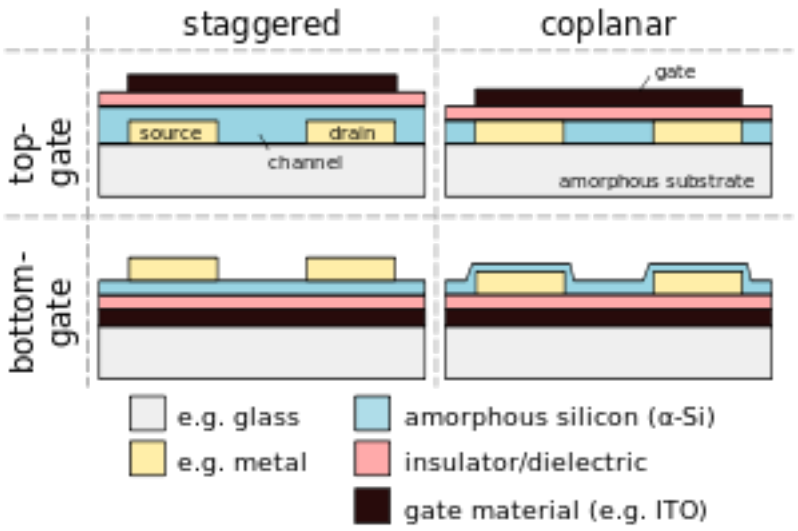

Figure 1.2: Types of TFT construction

If the TFT is top gate, then the substrate at the bottom can be non-conducting or if semiconducting, then it should have the opposite majority carrier from that of semiconducting channel within source-drain electrodes and in between dielectric layer & substrate.

If the TFT is bottom-gate with a non-conducting substrate, then a conducting layer needs to be deposited over it for gate contact, else a heavily doped semiconducting or a conducting substrate can be directly used both as support and also for gate contact terminal.

In case of staggered TFT for bottom gate, semiconducting channel is deposited prior to source-drain electrodes while it is reverse in case of top gate approach.

In case of coplanar TFT for bottom gate, semiconducting channel is deposited after and over the source-drain electrodes while it is reverse for top gate. Thickness of electrodes and semiconducting channel are almost same for a coplanar top-gate TFT.

1.3 High-k Dielectrics and Moore's Law

High- dielectrics are those materials which have a relatively high dielectric constant when compared to silicon dioxide as a reference. High- dielectrics are used in transistor manufacturing process where they are generally used to replace a silicon dioxide gate dielectric or another dielectric layer of a device. The drastic performance improvements in microelectronics over the past few decades have been accomplished by severe reduction in the size of memory and logic devices. In traditional MOSFETs, the Si-SiO_2 has been extensively used with silicon dioxide as the insulating or dielectric layer. Polysilicon gate and SiO_2 gate dielectric for the MOSFET devices has been widely used throughout MOSFET history till now. High quality of SiO_2 and its interface compatibility with silicon substrate was a crucial role in its development. SiO_2 grown in high temperature directly from the silicon possesses many desirable properties such as lower trap density, excellent interface quality, high thermal stability, thickness control ability and good reliability. The capacitance density (C/A) is directly proportional to k value and inversely proportional to thickness of the dielectric layer as given by the equation:

$$\frac{C}{A} = \frac{k\epsilon_o}{t_{ox}} \tag{1.1}$$

where t_{ox} and k are the thickness and relative dielectric constant of the high-k material respectively. Thus, miniaturization demanded the drastic decrease of the SiO_2 thickness to achieve much higher capacitance densities to get higher switching speeds. Fundamental limits of SiO_2 as a dielectric material, imposed by electron tunneling, will be reached as the film thickness approaches approximately 1 nm. This thickness is already at a level where severe problems start to occur because going much beyond reaches atomic level and properties start to differ drastically. At this small thickness, the dielectric

will not be able to effectively withstand even few voltages and hence tunneling current propagates along with the problem of physical stability and reliability of the film. The solution for the problems mentioned above, related to SiO2scaling down, is to select a gate dielectric with a higher dielectric permittivity than compared to SiO_2 (k = 3.9), that can provide a lower equivalent oxide thickness (EOT) at higher physical thickness. The implementation of high- gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as supporting the prediction of Moore's Law. So, it is this relevance of high-k dielectric materials that helps to achieve higher physical thickness and lower EOT to sustain Moores law prediction by reducing leakage current at much low dimension that was not possible with traditional silicon dioxide.

The following graph shows the trend as predicted by Moore, which is being traversed by various chips produced by different companies.

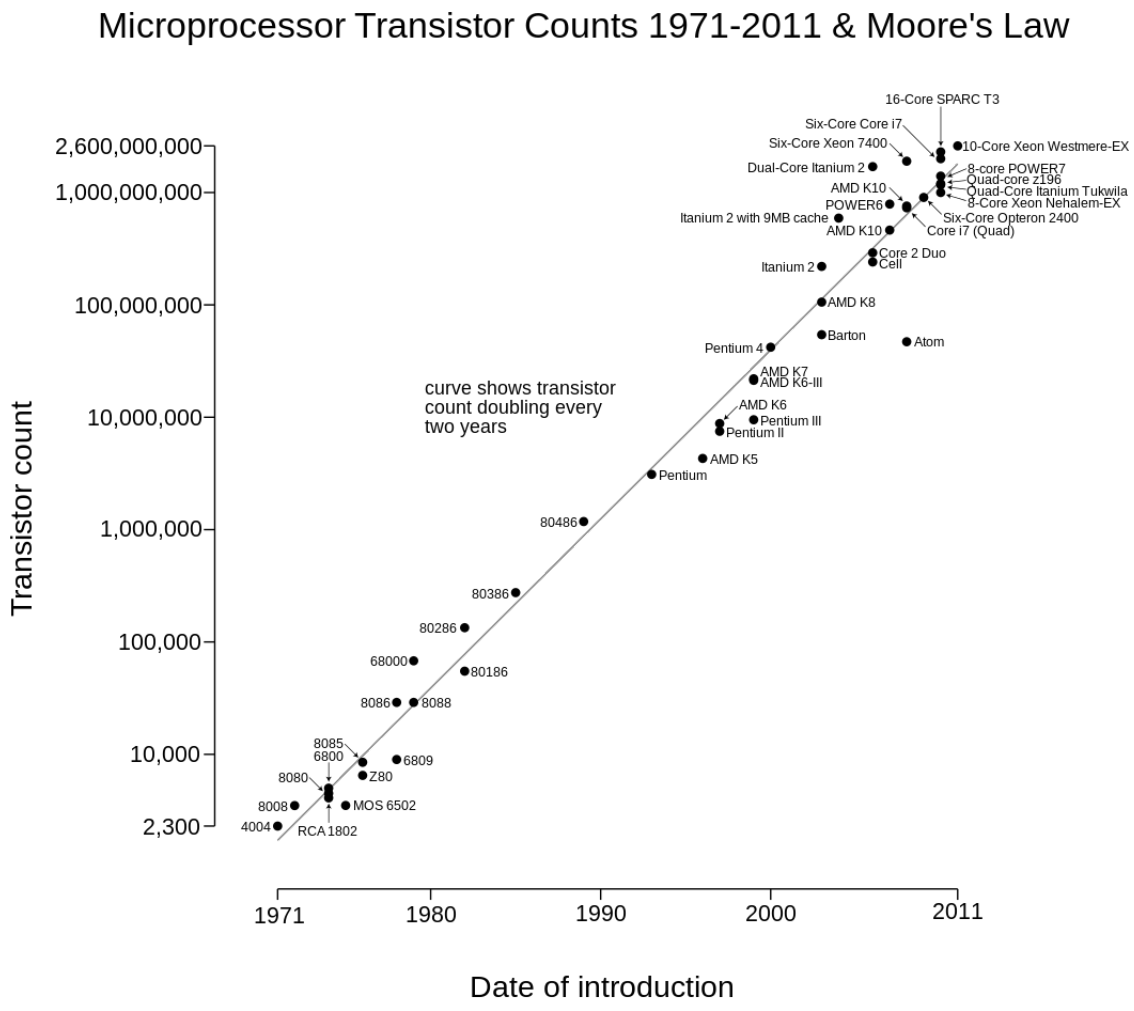

Figure 1.3: ICs following Moore's law trend

Moores law is in fact not a law but rather a prediction that the future trend will follow based on the past observations. This observation was made by the co-founder of Intel Corporation, Gordon Moore in 1965. He stated that the number of transistors per square inch on integrated circuits will double every year since the inception of integrated circuits. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down a bit, but data density has doubled approximately every 18 months, which is the current definition of Moore's Law. Most experts, including Moore himself, expect this prediction to hold for at least another one and half decades. The simplified version of this law states that processor speeds, or overall processing power

for computers will double every two years. This is all possible due to the advancement and precision in microelectronics fabrication technology. It is true that it will hold the prediction up to some timescale but it is going to deviate as we reach the limitations of high-k dielectric materials. So, researchers need to find much higher dielectric materials that can be compatible with the well-established silicon technology.

There are many properties that a high-k dielectric material should possess such as a large energy band gap and high barrier height with silicon substrate and metal gate in order to reduce harmful leakage current. It should have a large dielectric constant value and thermodynamic stability with silicon to resist the formation of a low-k SiO_2 interface. It should possess a high amorphous-to-crystalline transition temperature for sustaining a stable morphology post heat treatment. It must have low oxygen diffusion coefficients to prevent the formation of a low-k thick interface layer. It should have good channel carrier mobility, low fixed charge density, low defect densities, negligible C-V hysteresis and good reliability that can support a longer life time. Also, this high-k gate dielectric material should be compatible with present day CMOS fabrication process flowchart and other materials used in the CMOS integrated circuits.

In general, there are three types of high-k dielectrics:
1. Dielectrics with $4 < k < 10$ such as SiN_x
2. Dielectrics with $10 < k < 100$ such as HfO_2, Ta_2O_5, Al_2O_3, ZrO_2, etc.
3. Dielectrics with $100 < k$ such as PZT, BT, etc.

The type 2 dielectric film has been regularly used in transistors such as TFTs. The high-k dielectric material is usually used in combination with a high quality dielectric interface layer to lower the interface density of states. Numerous high-k materials ranging from k-values with 16-24 like HfO_2 to perovskites having k-value in the range of 102-104, are being actively investigated, in order to find a long term promising material. However, finding such a suitable high-k material is a major challenge because the selected material must me thermally stable, have a higher resistivity, act as a good barrier layer, and form an ideal interface with silicon. SiO_2 films can be conveniently grown by dry or wet oxidation of the silicon wafer. So, forming the oxide from its parent material is the biggest advantage and is one of the reasons why Si-SiO_2 system remained in IC industry for so long. However, high-k materials must be formed by deposition using physical vapor deposition (PVD) or chemical vapor deposition (CVD).

1.4 Equivalent Oxide Thickness

The equivalent oxide thickness (EOT) of a material is defined as the thickness of the SiO_2 layer that would be required to achieve the same capacitance density as the high-k material in consideration. EOT is thus given by:

$$EOT = \frac{3.9}{k} * t_{high-k} \tag{1.2}$$

where t_{high-k} is the thickness of the high-k dielectric material. This equation is derived by equating the capacitance densities in case of two devices, one with SiO2 as dielectric and the other with high-k dielectric material compared to silicon oxide.

$$\frac{C_{SiO_2}}{A} = \frac{k\epsilon_o}{t_{SiO_2}} \tag{1.3}$$

$$\frac{C_{high-k}}{A} = \frac{k\epsilon_o}{t_{high-k}} \tag{1.4}$$

Now, equating these two capacitance densities, putting the value of k_{SiO_2} as 3.9 and representing t_{SiO_2} as EOT, we get the equation for equivalent oxide thickness.

Now, high-k material obviously has k-value greater than 3.9, so the factor 3.9/k is less than unity. So, mathematically, one can see that we require a high value of t_{high-k} to get the same capacitance density that a much lower thickness of SiO_2 provided. This improvement in physical thickness helps in reducing the leakage that was exponentially increasing when t_{SiO_2} went below 2 nm. One needs higher capacitance density for sufficient polarization through the dielectric to produce high enough electric

field across oxide for efficient channel conduction and switching in the semiconducting layer between source and drain. For getting higher capacitance densities, one needs to reduce the oxide/dielectric thickness (as clearly observable from the equation) which again creates the problem of parasitic leakage. It is quite obvious that if one goes on reducing the high-k dielectric thickness, one can achieve an EOT well below 1 nm with much higher capacitance. So, research is needed to find an optimum thickness that produces desirable capacitance density but not at the cost of getting leakage that can hamper the device functioning. This can be called as a trade-off between lowering the thickness with a greed and desire for high capacitance density and increasing the thickness for hatred towards getting high leakage current. Thus, with the advancements of high-k dielectric materials compatible with silicon technology, it has been possible to achieve high capacitance densities and higher switching speeds that would have been possible with SiO_2 having a physical thickness much beyond 1 nm, which is in fact physically impossible to fabricate. Hence, these high-k dielectric materials are priceless gifts to overcome the saturation in the IC industry.

If there are dielectric stacks with different high-k materials or combination of SiO_2 with high-k dielectrics, one can use the capacitance density equation for capacitor in series arrangement and find out individual EOTs. And finally, the total equivalent oxide thickness is given by:

$$EOT_{tot} = t_{SiO_2}(if any) + EOT_1 + EOT_2 + EOT_3 + ... \tag{1.5}$$

1.5 Motivation for HfO_2

The choice of a material with higher dielectric constant compared to silicon dioxide can give the same equivalent oxide thickness with a higher physical thickness. Several high-k materials were identified suitable for gate oxide but many of them did not have all the desired properties. High-k materials under investigation include HfO_2, ZrO_2, Al_2O_3, Y_2O_3, CeO_2, Ta_2O_5, TiO_2, La_2O_3, and Nb_2O_5, etc. The dielectric constants of these grown films varies based on the deposition parameters and also on the type of deposition system such as pulsed laser deposition (PLD), RF Sputtering, atomic layer deposition (ALD), molecular beam epitaxy (MBE), etc. Searching and selection of the best high-k candidate is not an easy task as each of these materials does impart some challenges within the dielectric layer itself or compatibility with the silicon CMOS technology.

There are also problems if we aspire for very high-k dielectric materials as they can cause issues like the fringing field induced barrier lowering (FIBL). As the ratio of the dielectric thickness increases, the cross section of gate dielectric becomes a rectangular shaped rather than a sheet. This implies that the gate control would be severely affected by the field near source and drain area. Consequently, gate voltage can lose the modulation ability of channel carrier concentration and short channel effects get more fatal. Therefore, the threshold voltage (V_{th}) rolls off and the subthreshold swing gets worse. It is seen that the optical bandgap of dielectric is inversely proportional to dielectric constant. So, a very high dielectric constant material has a very small band gap resulting in small barrier height that has higher leakage current due to Fowler-Nordheim tunneling and faster breakdown strength. Hence, moderate dielectric constant materials with k-value in the range of 15-30 are preferred for further investigation.

1.6 Material properties of hafnium oxide

HfO_2 has a relatively high dielectric constant of around 22-25 and is thermodynamically stable in contact with Si which is the biggest advantage compared to other high-k dielectrics and has been adopted by Intel in its microprocessors recently. SiO_2 has relatively low dielectric constant of 3.9 and hence a very high optical band gap close to almost 9 eV. The observed optical bandgap of HfO_2 is 5.68 eV, which is lower compared to SiO_2 because of its high dielectric constant. But again, the dielectric constant value of HfO_2 is not that high enough and hence has proper barrier height that ensures a fairly low reasonable leakage current due to Fowler-Nordheim tunneling. Hafnias small lattice mismatch and similar thermal expansion coefficient with silicon makes ita more potential candidate for future gate dielectric. HfO_2 is expected to be highly resistive to the impurity diffusion because of its high density,

which is about 9.68 g/cm^3.One disadvantage associated with HfO_2 is the slight growth of a low-k interfacial layer between substrate and HfO_2. The following table compares the material properties between HfO_2 and SiO_2 :

Material Properties	HfO_2	SiO_2
Dielectric Constant	22 - 25	3.9
Bandgap (eV)	5.7	9
Density (g/cm^3)	9.68	2.27
Band offset for electrons	1.5	3.5
Band offset for holes	3.4	4.4
Lattice Constant (Å)	5.11	-
Lattice Mismatch with Si	close to 5%	-
Thermal Expansion Coefficient	5.3x10^{-6} K^{-1}	0.5x10^{-6} K^{-1}

Table 1.1: Comparison of material properties between HfO_2 & SiO_2

1.7 Motivation for ZnO

Zinc oxide is a quite multifunctional material that can be used in many microsystems and MEMS applications. During the last decade, the study of ZnO and its implication in micro-scale and nano-scale devices has grown in a proliferated fashion. Because of its unique optical, electrical and piezoelectric characteristics, its thin film has been widely used for variety of small scale devices. Specifically, piezoelectric property of ZnO has been used in numerous applications from filters and resonators to mass sensors and micro-actuators such as micro-pumps, micro-valves, etc. The conglomeration of its wide band gap, electrical, optical and piezoelectric properties makes it a unique candidate for a wide range of present and future device applications. It is one of the leading candidates for efficient signal transduction between electrical and mechanical domains in both sensors and actuators, due to its high electromechancial coupling coefficient. Other than ZnO thin films, needless to say, the recent advancements in nano-scale ZnO structures such as nanobelts, nanorods, and nanowires has incited new zeal into its future implementation. ZnO has also got applications in extreme conditions like nuclear reactors and space for its radiation hardness, i.e. high resistance to various hazardous radiations compared to other materials.

A saying in transistor arena goes like, One persons packaging nightmare is another persons sensor. This explains the fact that, during the fabrication of transistors for IC industry, i.e., computing applications, if there are difficulties in the final packaging of the chip, it is a waste and loss for that field but can be a boon for some other field such as the sensor industry since the semiconducting channel needs to be exposed to the ambient for conductivity change and doesnt require any protective packaging unlike IC applications. ZnO have been used as a sensing material for its high electromechanical coupling constant, high carrier mobility and sensitivity to current changes upon adsorption of foreign molecules on the surface of thin film. It has been used in gas sensors to detect gases like ammonia, methane, hydrogen, etc. FETs with ZnO thin film as semiconducting channel can be used as sensor as the channels work function and resistivity changes with time when analyte molecules adsorb on its surface.

1.8 Material properties of zinc oxide

Zinc oxide is generally found as hexagonal wurtzite and cubic zinc blende, of which wurtzite is more common as it is stable in ambient conditions. In its normal form, zinc oxide is an n-type semiconductor with electrons as the majority carrier because of residual donors. Pure microcrystalline ZnO is white but single crystal is colorless. It turns lemon yellow with heating and reverts back to white on cooling. It has a good resistivity control over the range of 10^{-3} to 10^5 -cm, high electrochemical stability, good chemical stability against hydrogen plasma and transparency in the visible range with a wide direct

bandgap of 3.37 eV or 375 nm at room temperature. Due to large band gap, it offers higher breakdown voltages, ability to sustain large electric fields, lower electronic noise, high-temperature and high-power operation. It is non-toxic and abundantly available in nature. Since it has high electrical conductivity and optical transmittance in the visible region of the electromagnetic spectrum, it is suitable for photovoltaic applications. Electron mobility varies strongly with temperature and its maximum value is approximately 2000 cm^2/ V-s at 80 K. Information on hole mobility is rarely available with values ranging from 530 cm^2/V-s. ZnO is a relatively soft material with high heat capacity, heat conductivity, low thermal expansion and high melting temperature. It has the highest piezoelectric tensor among the tetrahedrally bonded semiconductors. It is transparent to visible light but strongly absorbs UV light below 365 nm. The following table charts enlists some of the other properties of zinc oxide:

Material Properties	ZnO
Molecular Weight	81.37 g/mol
Relative Density	5.607
Vapor pressure at 1500^{o}C	12 mm
Heat Capacity	9.62 cal/^{o}C /mole at 25^o C
Coefficient of thermal expansion	4 x 10^{-6} / ^{o}C
Bandgap	3.37 eV
Hardness	4.5 on Mohs scale
Melting point	Sublimes at 1200^{o}C and 1975^{o}C at high pressure
Entropy	10.43 cal/^{o}C/mole
Refractive Index	2.0041

Table 1.2: Material properties of ZnO

Chapter 2

Fabrication Technology

This chapter outlines the technology and techniques associated with the fabrication process of the various devices, provides schematics of the device layouts and the experimental steps with process parameters.

2.1 Wafer cutting and Cleaning

Silicon wafers have got two cut marks namely primary cut and secondary cut where the angle between them is 90 degrees for p-type (100) silicon wafers. The following figure shows the cut marks for a p-type silicon. The wafers are cleaved along the primary or secondary cuts into smaller sizes of suitable

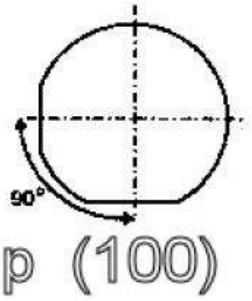

Figure 2.1: Wafer cuts for a p-type (100) silicon

substrate dimensions prior to a dedicated cleaning procedure required for fabrication of good quality thin films.RCA wafer cleaning procedure was concocted by Werner Kern and Puotinen of RCA, United States in 1965. RCA stands for Radio Corporation of America. Many derivatives of RCA cleaning procedures emerged with time but the basic connotation remains same. The derivative that was used for cleaning of silicon wafers starts with sonication in isopropyl alcohol, i.e. IPA-1,2 and 3 (3 being the last used), followed by acetone with rinsing in deionized (DI) water in between usage of two different chemicals. Hydrofluoric acid (HF) is used for the removal of native oxide layer. H_2SO_4+H_2O_2 (1:1) mixture is used for the removal of heavy metals and sometimes 3:1 mixture of these chemicals is used for the removal of oxide layer, which is called the Piranha solution.

2.2 Thin Film Deposition

The process of depositing thin films using specific sophisticated techniques on the substrate with some predetermined process parameters is called thin film deposition. There are certain properties of the substrate and thin films that decides the quality of thin film deposition and interface layer such as crystal orientation, thermal conductivity, thermal expansion, electrical resistivity, flexibility, flatness, thickness, etc. There are many applications of thin films such as microelectronics, thin film transistors, flat panel display sensors, actuators and detectors protective coating, decoration, antireflection coating

thin-film battery seed layer for nanostructures optoelectronics data storage microelectromechanical systems (mems) biotechnology photographic plate/mask. Hence research in thin film deposition is required to understand the modification of properties at the interface layer, scaling down of ICs and other microelectronic devices, to understand the adhesion and sticking coefficient with silicon wafer, for reduction in dimension and quantity of materials used which gives low cost devices. Thin film also provides ease of patterning circuits and various modification. One can deposit thin films using physical vapor deposition (PVD) and chemical vapor deposition (CVD). In the reported work, sputtering technique has been used for the deposition of HfO_2 and ZnO thin films because this technique has low thermal budget, less consumption of source materials, non-toxic effect, ease of handling and multi-target processing.

2.2.1 RF Sputtering

Sputtering is a PVD process in which atoms are ejaculated from a solid target material through momentum transfer by bombardment of the target by non-reactive (inert) energetic particles (ions). The target acts as the cathode which contains the source material that needs to be deposited. The substrate on which film is to be deposited acts as the anode, which is basically grounded along with the entire chamber to remain at a very low potential or zero with respect to the cathode. The chamber is also grounded so as to increase the anodic area so that potential drop gradient is too high. This is because area is inversely proportional to the voltage drop. As radio frequency (RF) is an oscillating frequency, if there is no voltage drop, then the flow of material might reverse such that material will come out of the substrate and get deposited on the target. The basic concept of cathode (target/source), anode (substrate) and momentum transfer are same for all sputtering systems but with slight difference in type of power source or design, we have the various types of sputtering systems such as DC sputtering, RF sputtering, Pulsed DC sputtering, Reactive sputtering, Magnetron sputtering, Bias sputtering, Ion sputtering, Co-sputtering.

Our laboratory has reactive magnetron RF sputtering with co-sputtering facility as well. The following figures show the schematic for a RF sputtering system for deposition of hafnium oxide and the image of the sputtering system present in our lab.

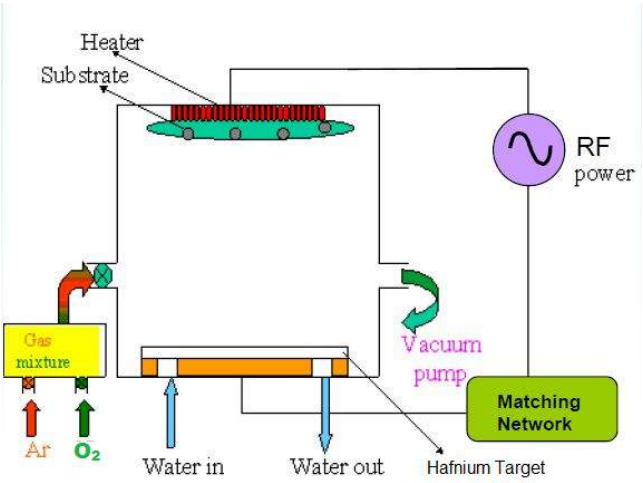

Figure 2.2: Schematic for sputtering of HfO_2

There are water circulation to cool the target as well as vacuum pumps associated in creation of high vacuum for chamber. An inert gas (e.g. Ar) is fed into the vacuum chamber of sputtering system at low pressure. A voltage is applied in between the two electrodes and a plasma is created. The plasma contains neutral argon atoms and roughly equal number of ions and free electrons. Hence, plasma is a conducting medium that contains a beam and array of particles that can be atoms, ions, molecules. The positive ions in the plasma are accelerated towards the negatively biased target. These energetic ions strike the target and dislodge (sputter) the target atoms through momentum transfer. These atoms are then free to travel through the plasma as a vapor and deposited on the surface of the

Figure 2.3: Image of reactive magnetron RF sputtering at NIT Rourkela

substrates due to the potential drop from target to substrate. The process parameters with which one can play in RF sputtering system are RF power, substrate temperature, target-to-substrate distance, gas flow ratio, time of deposition, pressure inside chamber during deposition, substrate rotation, substrate bias, etc.

2.2.2 Thermal Evaporation

It is a type of PVD process in which thin films are deposited by using evaporation of either solid or molten source. The source material is put inside a filament through which high current can pass to sublime and evaporate the materials towards the substrate. All these process happen inside a sealed chamber maintained at high vacuum. The filament must have high vapor pressure and much higher melting point compared to the source material. After getting a high vacuum in the range of 10^{-6} mbar, the filament was heated using electric current, in order to evaporate the aluminum source material and deposit it on the substrate. The following diagrams show a) schematic layout of the thermal evaporation system, and b)the thermal evaporation system of our laboratory:

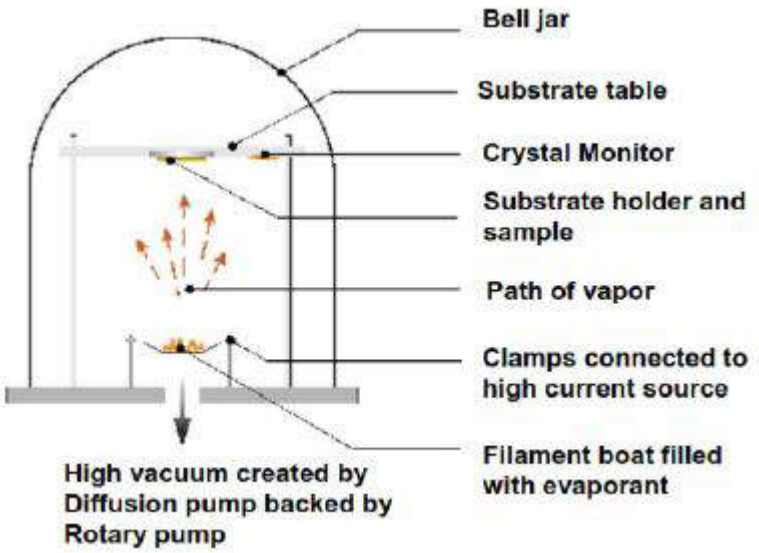

Figure 2.4: Schematic of Thermal Evaporation System

Figure 2.5: Image of Thermal Evaporation System at NIT Rourkela

2.3 MOS Device Layout

A dielectric oxide layer is stuffed in between a semiconducting layer and metal electrodes. The global aluminum layer at the bottom is for taking contact from the terminal of the other end.

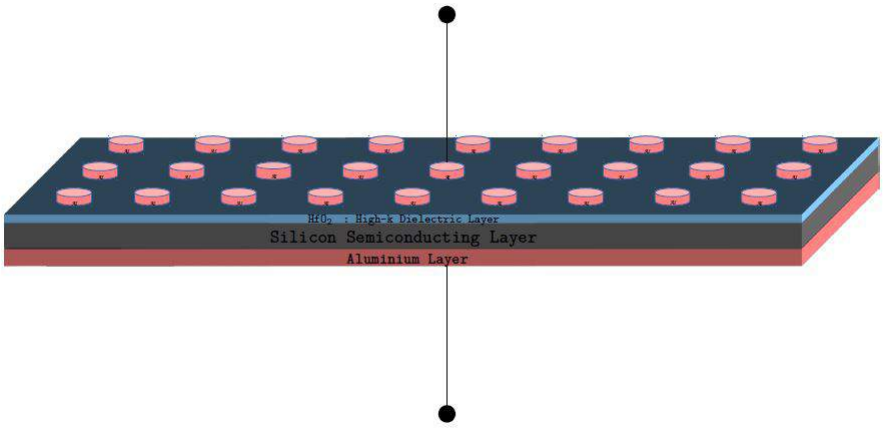

Figure 2.6: Layout of MOS device

2.4 MIM Device Layout

A dielectric oxide layer is clubbed in between two metals of which one side is the gate layer and the other end has metal electrodes. This MIM device is experimented with three different type of gate

materials for three different oxide thicknesses.

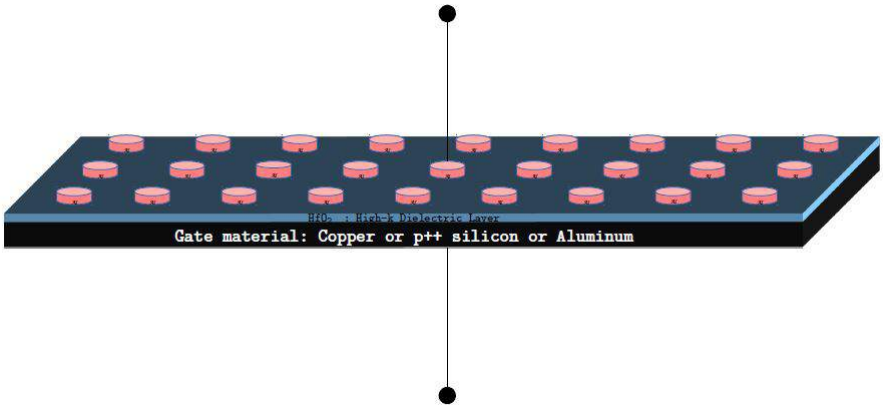

Figure 2.7: Layout of MIM device

2.5 TFT Device Layout

The following figures show the TFT device layout with three different gate materials. S, D and G representing the source, drain and gate terminals respectively.

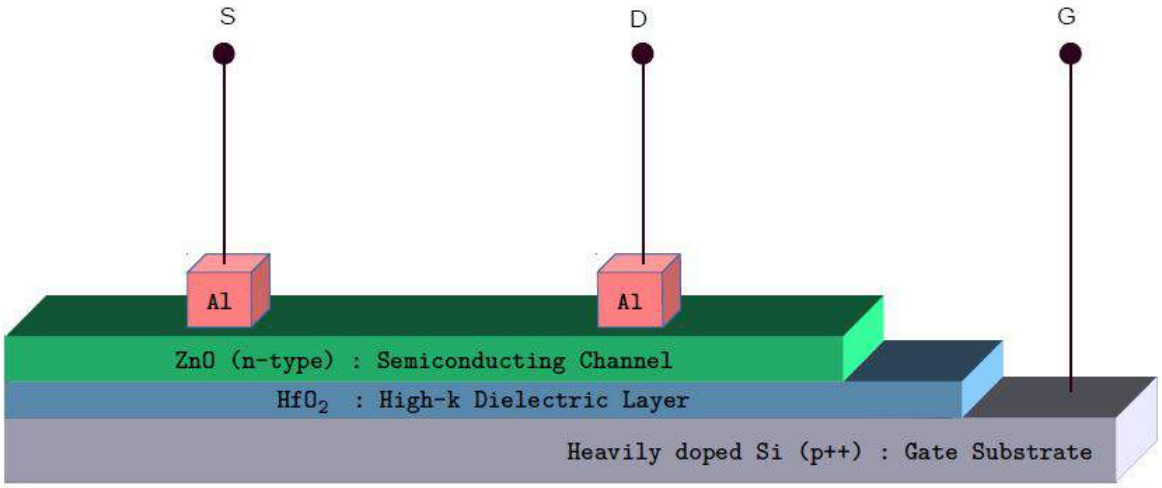

Figure 2.8: Layout of TFT device with p^{++} silicon as gate material

2.6 Experimental

The p-type silicon wafer was cleaved to get small substrates for the design of pMOS device. Similarly, heavily doped p++ silicon was cleaved for the design of MOSFET device. These silicon based substrates were thoroughly cleaned using the derivative of RCA cleaning process as mentioned in section 2.1. Also, copper substrates and glass substrates were cut from their pure parent material and thoroughly cleaned before the fabrication of MIM and FET structures with copper and aluminum as gate material. Copper and p_{++} silicon substrates were directly used as gate terminal and aluminum thin layer was deposited on glass substrates to be used as gate.

A global aluminum layer was deposited on the glass substrates using thermal evaporation of pure grade aluminum. The lowest chamber pressure achieved was $1.8\text{x}10^{-6}$ mbar. Hafnium oxide thin

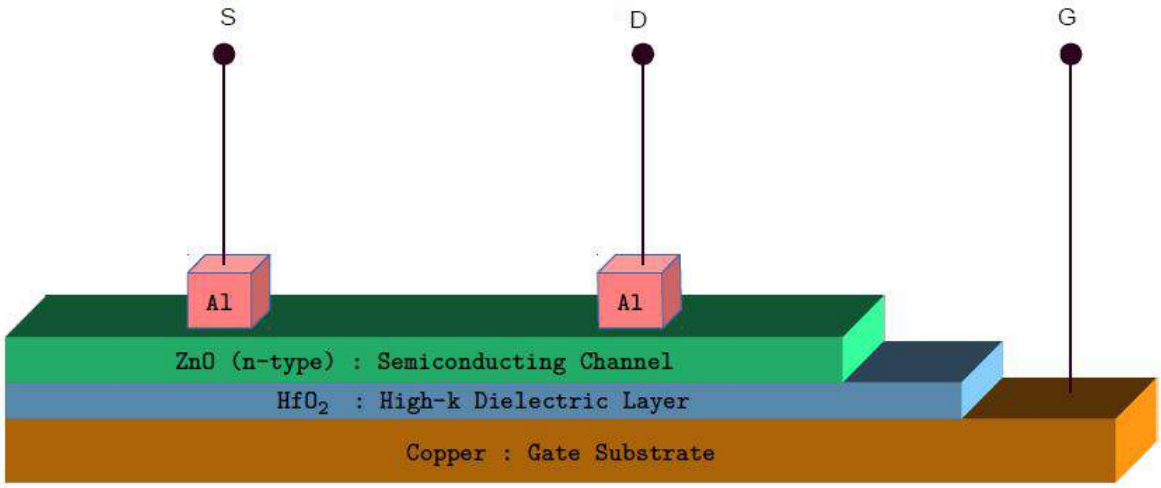

Figure 2.9: Layout of TFT device with copper as gate material

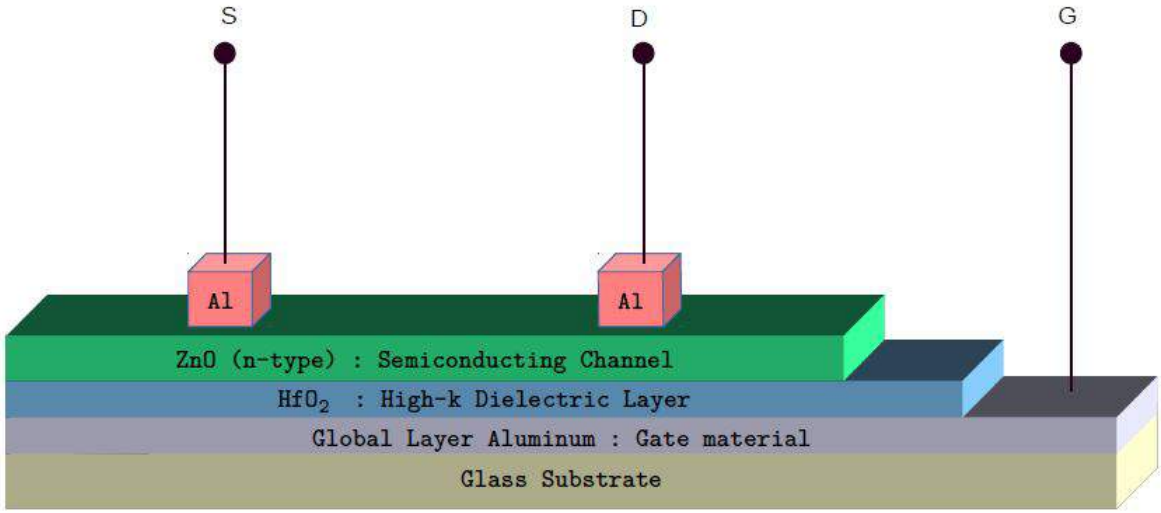

Figure 2.10: Layout of TFT device with aluminum as gate material

films were deposited on all the substrates using reactive magnetron RF sputtering of a pure grade HfO_2 target with a RF power 150W, gas flow ratio of argon:oxygen as 3:2, substrate temperature at room temperature and chamber pressure during deposition at 4.0x10^{-3} mbar. The target to substrate distance was kept fixed at 10 cm and the growth duration was varied according to the thickness of hafnia thin film desired. X-ray diffraction and UV-Visible spectroscopy was done for the hafnia films deposited on p-type (100) silicon substrate.

Zinc oxide thin semiconducting channel was deposited on the samples relevant for FET, using reactive magnetron RF sputtering of a pure zinc target along with flow of pure oxygen with a RF power of 150W, gas flow ratio of argon:oxygen as 2:3, substrate temperature at room temperature and chamber pressure of 8.0x10^{-3} mbar during deposition. The duration of deposition was decided based on thickness of semiconducting channel layer required. X-ray diffraction was done for ZnO thin film on p-type (100) silicon substrate.

Finally, the contact terminals were made by metallization using masks in a thermal evaporation system. A mask with circular apertures having diameter 1 mm was used for deposition of aluminum metal as contact terminals in case of MIM and MOS structures. A characteristic mask having source-drain terminals with a channel length of 500 μ m was used during metallization using pure grade aluminum by thermal evaporation system for the last stage in the fabrication of bottom-gate staggered

TFT device. The lowest chamber pressure achieved was $3.2\text{x}10^{-6}$ mbar. The source-to-substrate distance was kept fixed at 15 cm for all work in thermal evaporation system.

Chapter 3

Characterization techniques

3.1 X-Ray Diffraction

This is one of the most powerful techniques used for structural characterization of a sample in the scientific and industrial community. Since the properties of the material at macroscopic level gets changed because of even a minor modification at the sub-microscopic domains like nano- range or atomic level, hence, it becomes highly essential to know about the structural arrangement at the atomic level. When a beam of X-ray photons strike the sample, they undergo diffraction if they meet the condition of Braggs law:

$$2dsin\theta = n\lambda \tag{3.1}$$

where;
d = distance between interatomic lattice planes
λ = wavelength associated with the X-ray photons
n = order of diffraction
θ = angle of incidence with respect to the atomic plane

X-ray diffractometers consist of three basic elements such as the X-ray tube, a sample stage and the detector. X-ray photons are produced in a cathode ray tube by heating a filament to produce electrons by thermionic effect which are accelerated towards a target by applying a potential difference in order to bombard/strike the target material. When electrons have sufficient energy to dislodge/knock-off inner shell electrons of the target material, characteristic X-ray spectra is generated. The most common spectra produce are those of K_α and K_β. These specific wavelengths are characteristic to the target material. For production of monochromatic X-ray photons needed for diffraction, filtering is necessary by crystal monochrometers or foils. Copper is the most common target material with K radiation at 1.5418 Å. These X-rays are collimated and channelized to fall onto the sample. As the sample and detector are rotated, the intensity of the reflected X-rays is recorded. When the geometry of the incident X-rays impinging the sample satisfies the Bragg Equation, constructive interference occurs and a peak in intensity occurs. A detector records and processes this X-ray signal and converts

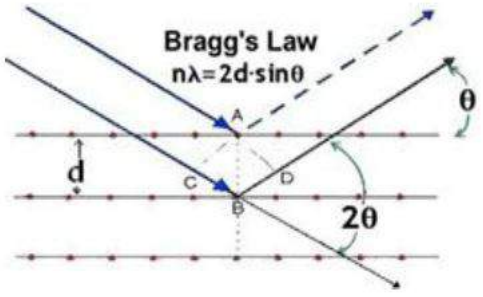

Figure 3.1: Schematic of the diffraction through crystal's atomic planes

Figure 3.2: Full view of the Rigaku Ultima IV from outside

the signal to a count rate which is then output to a device such as a printer or computer monitor. The geometry of the diffractometer is such that the sample rotates in the path of the collimated beam at an angle θ while the detector is mounted to collect the diffracted X-ray photons rotating at an angle of θ. The instrument used for rotating the sample and controlling the angle is called as goniometer.

3.2 UV-Vis Spectroscopy

UV-Visible spectroscopy refers to an optical method used to characterize the properties of a material using absorbance, reflectance or transmittance spectroscopy with photons in the ultraviolet to visible range. In this region of the spectrum, molecules generally undergo electronic transistions. The Beer-Lambert law states that the absorbance by a solution is directly proportional to the concentration of the absorbing species in the solution and the path length. Hence, UV-Vis spectroscopy can be used to determine the concentration of the absorber in a solution for a fixed path length. It is essential to know how fast or slow does the absorbance change with concentration. This is given by:

$$A = log_{10}(\frac{I_o}{I}) = \epsilon cL \tag{3.2}$$

where;
A = Measured Absorbance
I_o = Intensity of Incident Light
I = Transmitted Intensity
L = Path Length through the sample
c = Concentration of Absorbing species
We can also calculate band gap of the thin film from UV-Visible spectroscopy using the relation:

$$\alpha(\nu)h\nu = B(h\nu - E_{gap})^m \tag{3.3}$$

where;
E_{gap} = optical band gap
$h\nu$ = incident photon energy
B = constant ; m = 0.5 for direct band gap & 1 for indirect band gap
$\alpha\ (\nu) = \frac{2.303*Abs(\lambda)}{d}$ is absorption coefficient using Beer-Lambert's law
Abs(λ) = film absorbance and d = film thickness

3.3 Thin Film Thickness Measurement

The measurement of thickness of thin films lies at the root of any investigation related to thin film technology since thin film is almost a 2-D structure, the dimensions across length and breadth doesnt

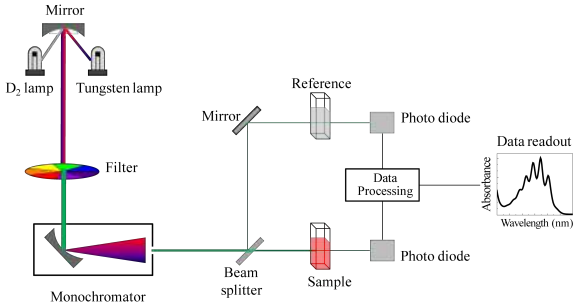

Figure 3.3: Schematic diagram of a UV-Visible spectrometer

make much difference but a slight change in the third dimension, i.e. height creates a significant change in the properties. There are basically two modes in which we measure the thickness of thin films such as contact mode and optical mode.

3.3.1 Contact mode

Contact mode measurement is basically done by stylus profilometer that measures the thickness and roughness by monitoring the deflections of a highly fine tipped cantilever called stylus, when it is dragged along the surface of the film. Stylus instruments are limited in speed and accuracy and hence are low cost equipments compared to their optical counterparts. They require a step, i.e. a considerable change in the height of the film to measure thickness. This method is usually preferred while measuring opaque films, such as metals.

3.3.2 Optical mode

Optical mode determines thin-film thickness by measuring how the thin films interact with light. These techniques can measure the thickness, roughness, and optical constants of a film that elucidate how light propagates through and reflects from a material. Once these optical constants like n (refractive index) and k (attenuation/extinction coefficient) are known, they may be related to other material parameters like composition and band gap. Optical mode is mostly preferred for measuring thin films as it is an accurate, nondestructive technique and requires little or no sample preparation. It also requires no step formation unlike contact mode of stylus profilometer. The two most common optical thin film thickness measurement types are spectral reflectance and ellipsometry. Spectral reflectance probes and measures the amount of light reflected from a thin film over a wide range of wavelengths with the incident light normal or perpendicular to the sample surface. Ellipsometry is similar to spectral reflectance except for the fact that it measures reflectance at non-normal or oblique incidence and at two different polarizations. So, it is quite obvious that spectral reflectance is much simpler and less expensive than ellipsometer, but it is restricted to measure less complex structures only.

3.4 Probe Station and Electrical Characterization

Probe station is that safe black box devoid of external noise and vibrations and has micro probe needles connected through special wiring to electrical characterization measurement apparatuses. This station has a system which helps to place the samples held firmly by very low vacuum so that one can direct the probes to requisite places on the sample and then take reading. It also has a hot oven beneath that can heat the sample while taking readings. This is attached to a PID controller to monitor the temperature.

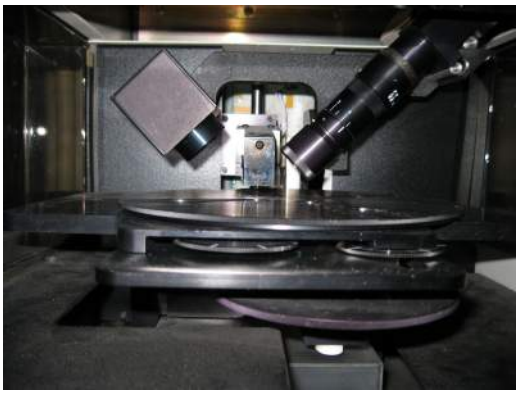

Figure 3.4: Stylus Profilometer

Figure 3.5: Ellipsometer

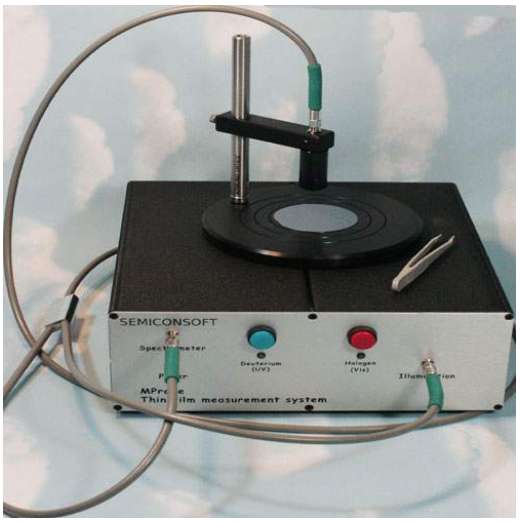

Figure 3.6: Spectral reflectance instrument

3.4.1 C-V Measurement

C-V measurement refers to the capacitance versus voltage measurement of electronic materials and devices. In the semiconductor devices technology, this measurement is highly essential for the critical task of maintaining the quality and reliability of gate oxides in MOS structures. C-V measurement is mostly used for studying the gate oxide in detail. These measurements are made on the two terminal devices called MIS/MOS capacitor and MIM/MOM capacitor to study various properties related to the insulating/dielectric layer. They provide abundant device and process information including bulk and interface charges. We use Agilent E4980A (20Hz-2MHz) Precision LCR meter in our lab for C-V measurement purpose.

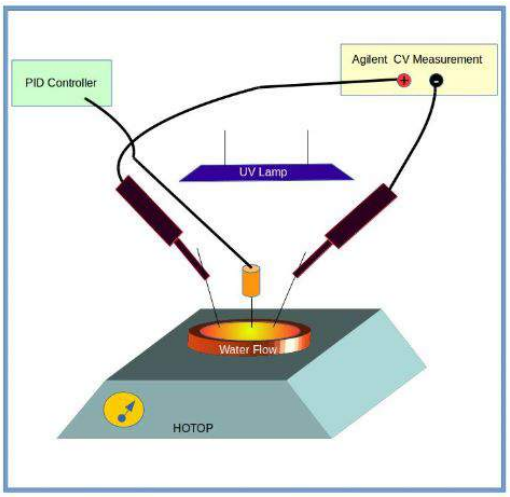

Figure 3.7: Schematic view of the system inside probe station

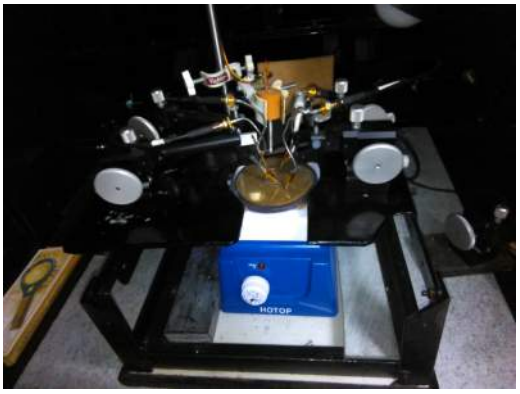

Figure 3.8: Image of the probe station set up used for the experiment

Figure 3.9: Electrical characterization instruments

MOS Capacitor

The MOS capacitor lies at the heart of any MOSFET device. So, before developing the FET device, it is essential to study the MOS properties to understand the behavior of the oxide dielectric. One may also say that MOS capacitor is basically a MOSFET without source-drain terminals. The C-V measurement helps in determining many MOS device parameters like oxide thickness, oxide capacitance, flatband capacitance, doping density, doping profile, depletion depth, metal-semiconductor work function difference, Debye length, threshold voltage, interface trap density, bulk potential and effective oxide charges.

C-V measurements in MOS devices are made using two simultaneous voltage sources such as applied AC voltage signal and a DC voltage that is swept over time. Magnitude and frequency of

the AC voltage are kept constant and magnitude of DC voltage is swept over time. The purpose of this DC voltage is to allow sampling of the device material at various depths while AC voltage bias provides a small signal bias such that capacitance measurement can be performed for the device at a particular depth. The oxide layer is sandwiched between the two plates, one made of semiconducting bulk and the other as metal gate, the area of which defines the effective area for the capacitor that would be needed for all calculations. During the operation of C-V measurement, three regions are formed such as accumulation, depletion and inversion.

A p-type semiconductor has holes as majority carriers in the valence band when no voltage is applied. More holes will appear in valence band at metal-semiconductor interface when a negative voltage is applied because negative charge with metal causes a net equal positive charge to accumulate at the interface between semiconductor and oxide. This state is called accumulation and oxide capacitance is measured in strong accumulation region for a p-type MOS capacitor. The capacitance is almost constant in this region and the oxide capacitance is calculated in the strong accumulation region, from which oxide thickness can be extracted.

The majority carriers are replaced from the semiconductor-oxide interface when a positive voltage is applied. This state is called depletion as the surface is depleted of majority carriers. In this state, the semiconductor acts as a dielectric or becomes an insulator because it can no longer conduct charge or contain charge. Thus, the oxide capacitance and depletion layer capacitance in series combination gives the total measured capacitance implies the measured capacitance decreases.

When the gate voltage of this p-type MOS capacitor goes beyond the threshold voltage, dynamic carrier generation and recombination takes place and electron-hole pairs are generated due to the positive gate voltage which attracts minority carriers, i.e. electrons towards the gate. These minority carriers accumulate at substrate-oxide interface since the oxide is a good insulator. Since the polarity is inverted in the accumulated minority carrier layer, it is called the inversion layer. Most available minority carriers are in inversion layer above a certain positive gate voltage and thus, further increase in gate voltage doesnt deplete the semiconductor, implies the depletion region reaches a maximum depth. The total capacitance measured is series combination of oxide capacitance and maximum depletion capacitance. The capacitance in inversion region at maximum depletion depth depends on measurement frequency due to which appearances of C-V curves vary at different frequencies and is more significant in lower frequency range.

MIM Capacitor

MIM capacitor is simply a metal-insulator-metal based parallel plate capacitor in which the dielectric is sandwiched between two metallic layers. The effective area of the capacitor is the area of the mask used in metallization of the top electrode. Basically, the capacitance shall remain almost constant in some voltage range. From the known capacitance density and thickness of dielectric film, one can calculate the dielectric constant of the oxide layer. Calculating this dielectric constant becomes highly essential because we have known the importance of high-k dielectrics, Moores law and equivalent oxide thickness in Chapter-1.

3.4.2 I-V Measurement

Keithley6487 Picoammeter was used for all the two terminal I-V characterization and Scientech 4073 DC power supply to supplement for the three terminal I-V measurements. There are various types of trap centers in the bulk as well as interface that can help leakage such as interface trapped charge, oxide trapped charge, fixed oxide charge and metal oxide charge. The presence of defects can also lead to a leaky pathway that can assist leakage current. There are various types of electronic conduction and tunneling mechanisms. The intrinsic carriers cause a conduction in ohmic type with high resistivity but the extrinsic carriers that can travel freely within the oxide layer cause conduction through Schottky effect, Direct tunneling and/or Fowler-Nordheim tunnel effect. The extrinsic carrier transport assisting in leakage while in association with traps can be through Frenkel-Poole effect, Hopping conduction or Space-charge limited current.

MOS Capacitor

There can be leakage at the metal oxide interface, oxide-semiconductor interface as well as semiconductor-metal contact. All these factors contribute towards the I-V characteristics of the MOS capacitor. Some or all of the types of electronic conduction pathways can occur at these interfaces and within bulk while given voltage. These properties are quite temperature and frequency dependent also rather than only voltage. Based on the asymmetric nature in the accumulation and inversion biases, one may predict if the leakage current density is larger for gate injection or substrate injection for the same voltage value.

MIM Capacitor

Since we have a dielectric/insulating layer sandwiched between two metallic terminals, literally, there should be no current flowing in between them in ideal case as the electric field inside the dielectric is zero but there is always some few traces of current that pass through. Measuring this will help us understand the quality of dielectric film and can predict the order of leakage when the exactly same dielectric with same thickness shall be used in a FET. Dielectric breakdown and loss can occur at a high voltage range. So, we need to understand the operating voltage range for a particular thickness of dielectric. Here also, the gate injection can depend on temperature and some of the electronic conduction pathways through the oxide dielectric can take place as discussed in section 4.5.2.

MOSFET Output Characteristics

Output characteristics is one of the most important electrical characterization needed to understand the operation and quality of a transistor. We measure the current produced between source and drain terminals by sweeping the voltage in between them while keeping the gate biased. So, we measure I_{ds} versus V_{ds} keeping V_{gs} constant. This provides us the saturation region and non-saturation region or the flat region and linear region. If the channel length is less and carrier mobility is higher, then the linear region will fall within a very short voltage range and very quickly follow saturation. Simultaneously measuring I_{gs} versus V_{gs} can help in judging if the leakage is contributing to the channel conduction or not, i.e. we can know how much significant is the contribution of I_{gs} towards I_{ds}.

MOSFET Transfer Characteristics

Transfer characteristics is another important electrical characterization to understand the operating range and switching of the transistor. We measure the current produced between source and drain terminals by sweeping the voltage in between the source and gate terminals while keeping the voltage biased in between the source and drain terminals. So, we measure I_{ds} versus V_{gs} keeping V_{ds} constant. $I_{on}/\ I_{off}$ provides the on-off ratio and if this ratio is higher, we have a higher switching speed and vice-versa. It also gives the V_{th} i.e. threshold voltage, the value of V_{gs} from which the transistor can operate or switch on. This characterization method is quite vital if the transistor is to be used as a sensor and studying the channel current versus time response.

Chapter 4

Results and Discussion

This chapter provides the results from structural and optical characterization of the thin films along with electrical characterization results from MOS, MIM and FET devices in a graphical way and comparison in terms of change in gate material and thickness of dielectric layer. These characterization results are highly essential to change the fabrication process parameters required for optimization.

4.1 Structural Characterization

The following structural characterization through X-ray diffraction data confirms the presence of amorphous hafnium oxide thin film layer on silicon (100) substrate.

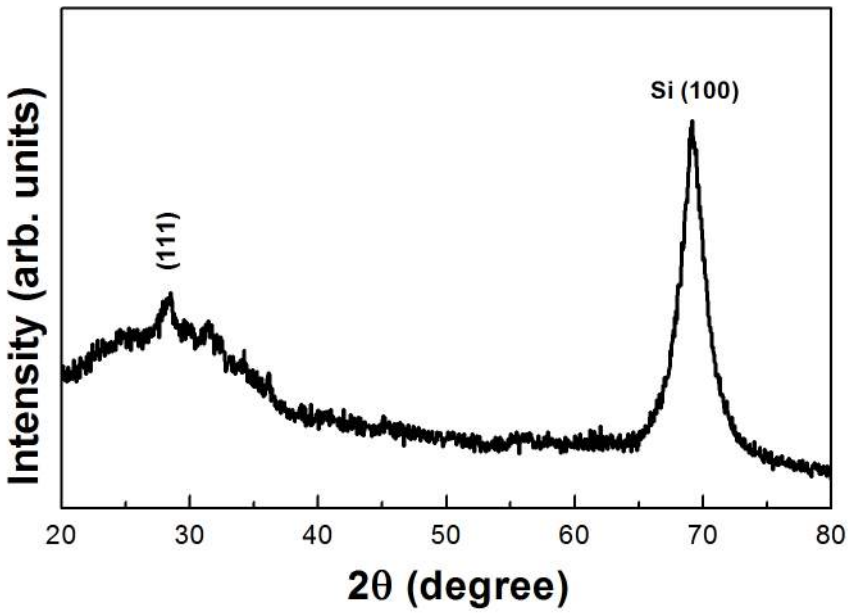

Figure 4.1: XRD of Hafnium oxide thin film

The following graph shows the crystalline peaks obtained for zinc oxide thin film that was fabricated with the same process parameters that would be used while deposition of the semiconducting channel in FET. The miller indices for the major crystal planes are (002) and (103).

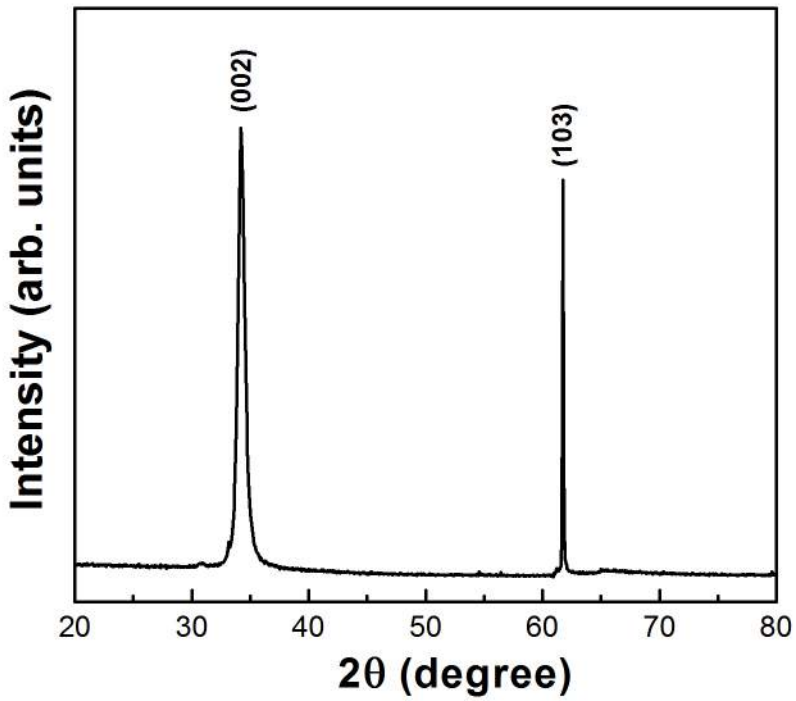

Figure 4.2: XRD of ZnO thin film on p-type (100) Si substrate

4.2 Optical Characterization

The following spectroscopic pattern is obtained from the UV-Visible spectrometer for the hafnium oxide thin film on silicon substrate. The wavelength at which maximum absorption occurs is 198.56 nm.

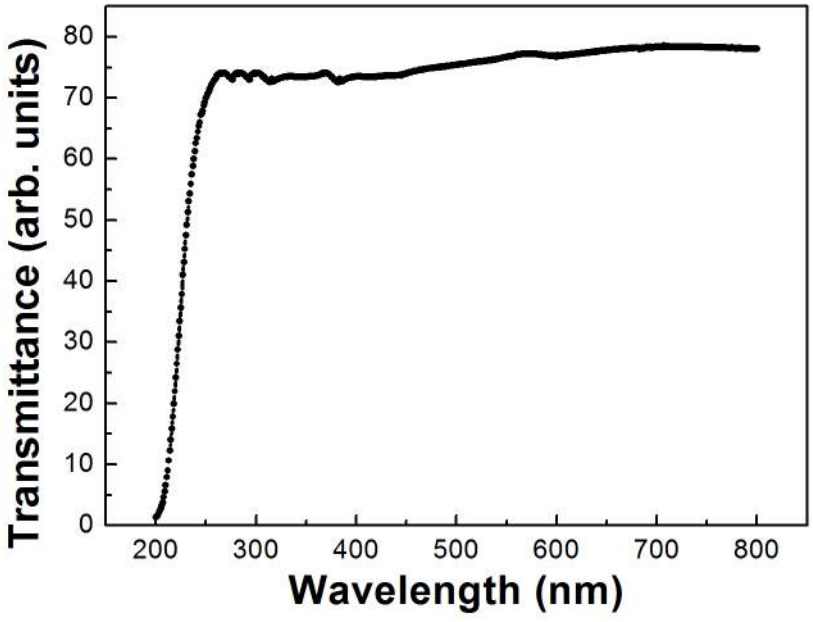

Figure 4.3: Transmittance spectroscopy from UV-Visible spectrometer

The following plot is required for the calculation of band gap of the thin film from the transmittance spectroscopy obtained by UV-Visible spectrometer as discussed in section 3.2 . The linear fitting is extrapolated to intercept the x-axis at 5.72 eV, which gives the band gap for HfO_2 thin film.

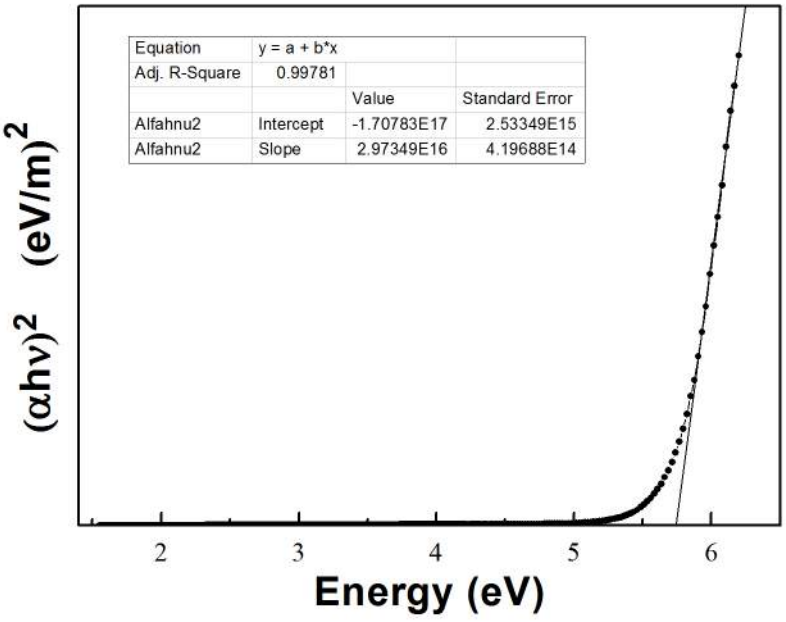

Figure 4.4: Band gap calculation of HfO_2 thin film from spectroscopic data

4.3 Electrical Characterization

The following plots portray the C-V and I-V measurements for the MOS structure. We can clearly depict the accumulation, depletion and inversion region in the C-V diagram. The Cox is found to be 379.18 pF, intrinsic Debye length of 4.171 nm, flatband capacitance of 189.57 pF and flatband voltage at -1.87 V.

From the linear fitting in $1/C_2$ plot above and with extrapolation and interception on x-axis, built-in voltage was found to be V_{bi} = -2.92 volt. Some other parameters were calculated such as substrate doping concentration N_{sub} to be 5.4463x 10^16 cm^{-3}, metal-semiconductor work-function as -1.709 eV, bulk potential as -0.284 eV, Q_{eff} as 9.236x10^{-9} C and N_{eff} as 5.765x10^{10} ions/cm^2.

The following graphs show the C-V and I-V curves for the MIM structure with copper as gate material with three different thickness of oxide dielectric.

It is quite evident from the graphs that the capacitance of the MIM structures decrease with increase in thickness of insulating layer but there is not a huge variation with thickness as we got mean capacitances of 7.89 pF, 7.63 pF and 7.60 pF for 20 nm, 30 nm and 40 nm layer of HfO_2 respectively. Also, it can be observed that the current flow through dielectric is much higher for lowest thickness of 20 nm and least for the thickest layer of 40 nm.

The following graphs show the I-V and C-V curves for the MIM structure with aluminum as gate material deposited on glass substrates for three different thickness of oxide dielectric.

With aluminum as gate material, we got mean capacitances of 7.24 pF, 6.88 pF and 2.61 pF for 20 nm, 30 nm and 40 nm layer of HfO2 respectively. There is considerable loss in capacitance while

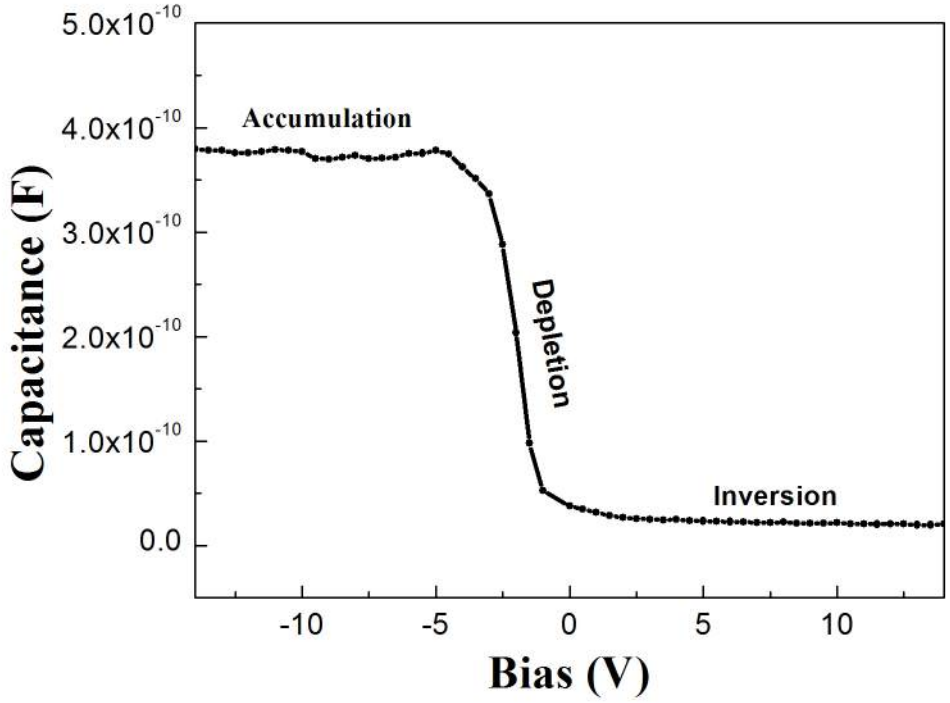

Figure 4.5: C-V plot of MOS

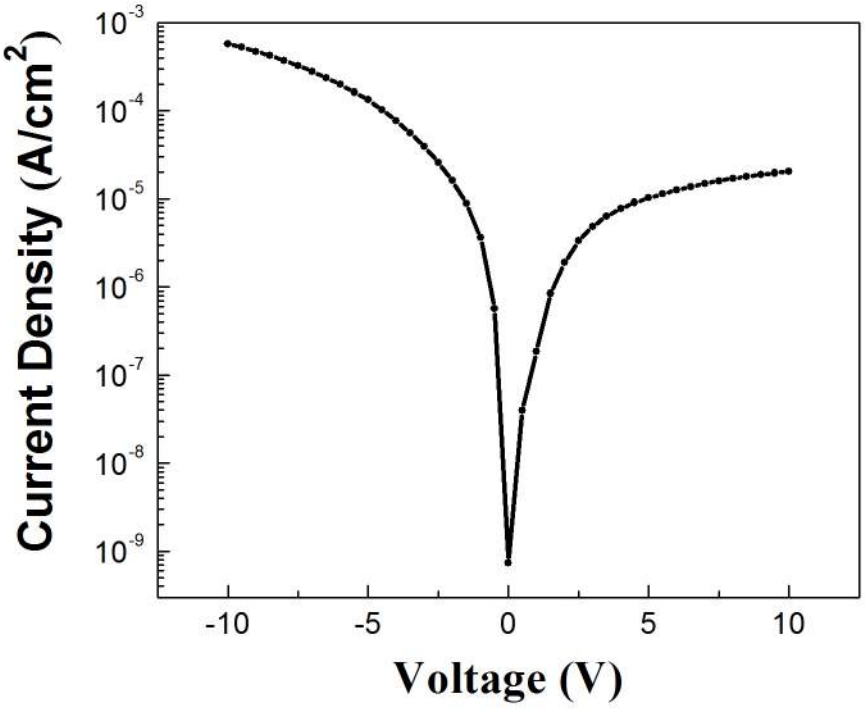

Figure 4.6: I-V plot of MOS

going from 30 nm to 40 nm. And, as obvious, again the current flow is much higher for low thickness and vice-versa. The quasi static region for current observed is much less flat compared to copper as gate material.

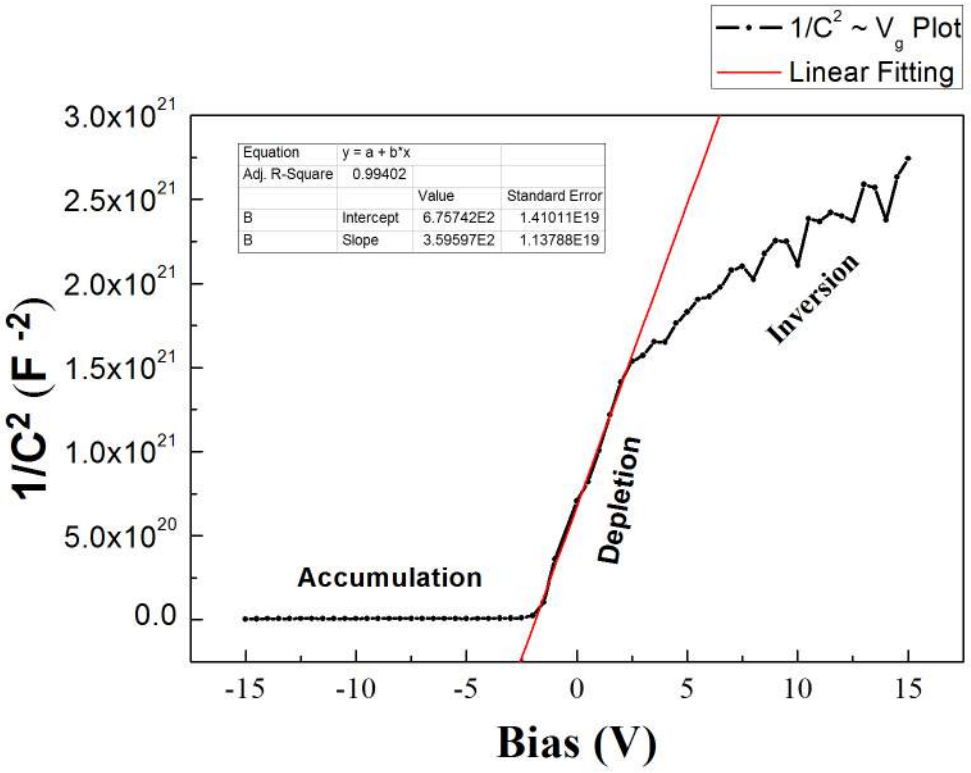

Figure 4.7: Inverse C squared versus voltage bias curve

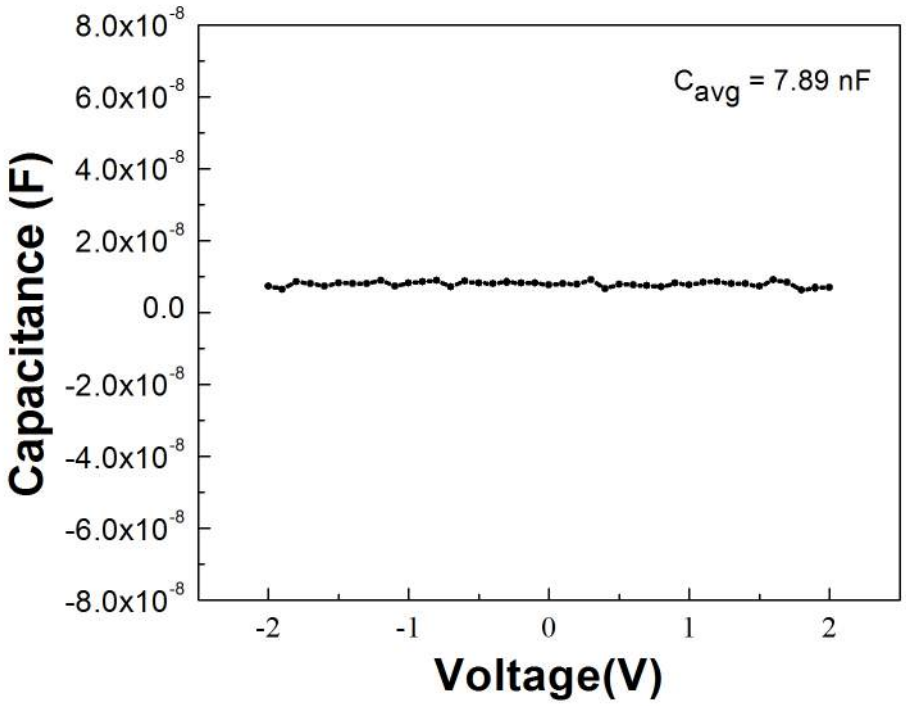

Figure 4.8: C-V plot for 20 nm hafnium oxide

The following graphs show the I-V and C-V curves for the MIM structure with heavily doped p^{++} silicon as gate material for three different thickness of oxide dielectric.

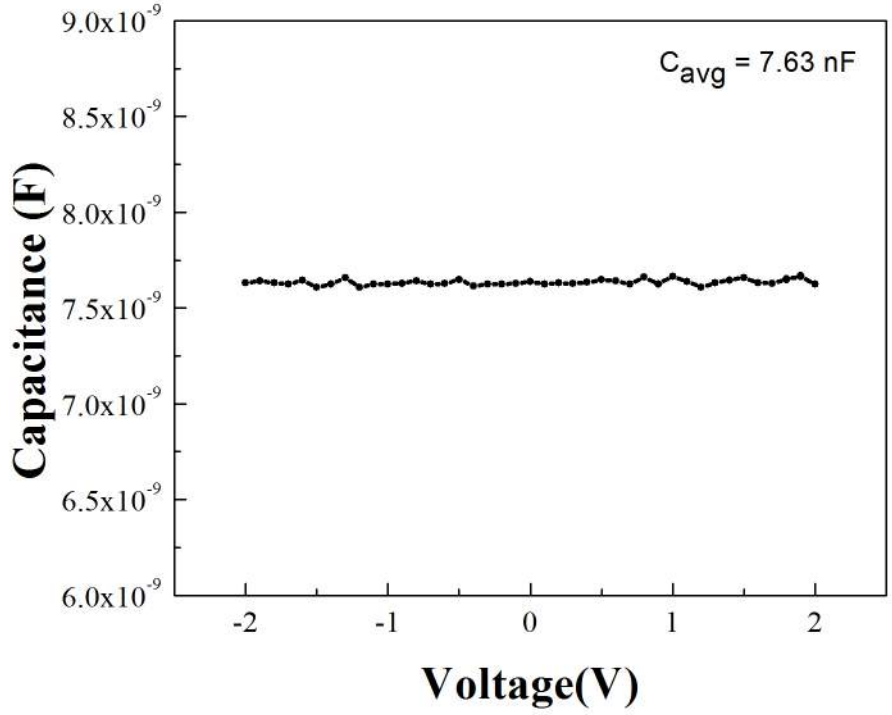

Figure 4.9: C-V plot for 30 nm hafnium oxide

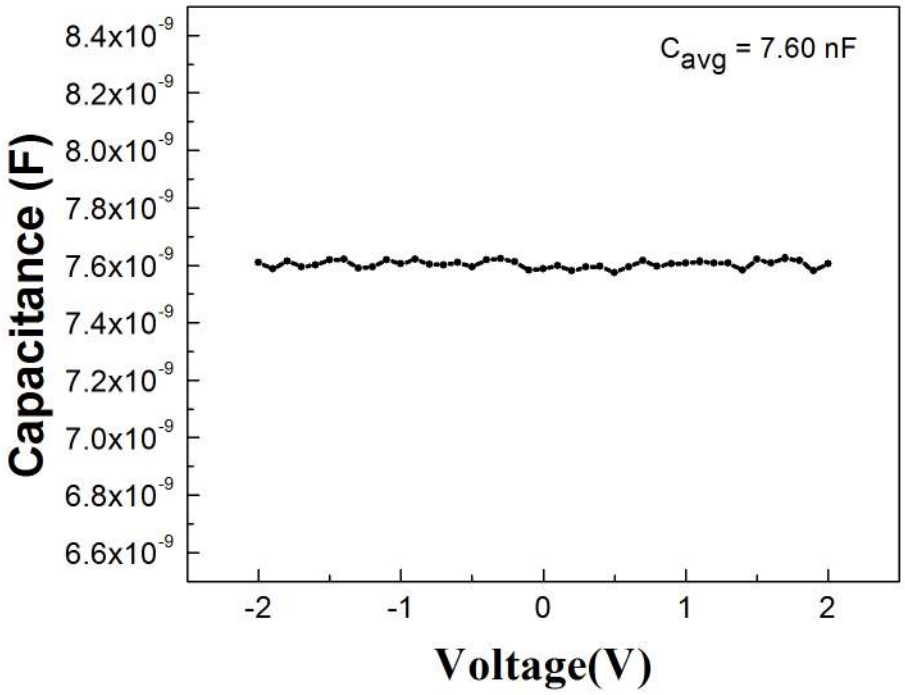

Figure 4.10: C-V plot for 40 nm hafnium oxide

Capacitances of 95.6 nF, 46.01 nF and 12.01 nF for 20 nm, 30 nm and 40 nm layer of HfO_2 respectively with p++ silicon as gate material. Thus, we are able to find much higher capacitance density in this case compared to copper and aluminum gate materials. The quasi static region for current is

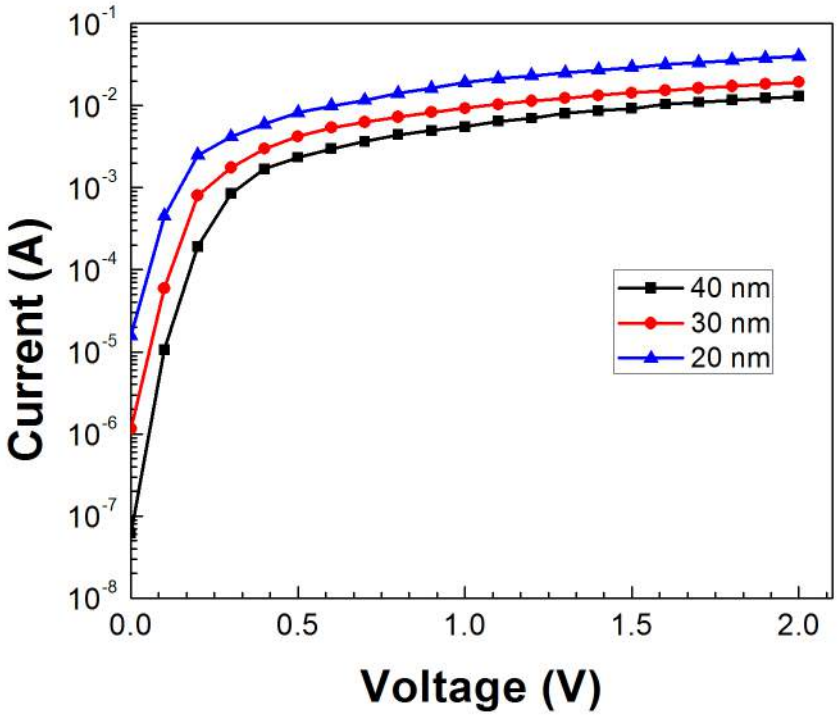

Figure 4.11: I-V of MIM structure with Cu as gate for different dielectric thickness

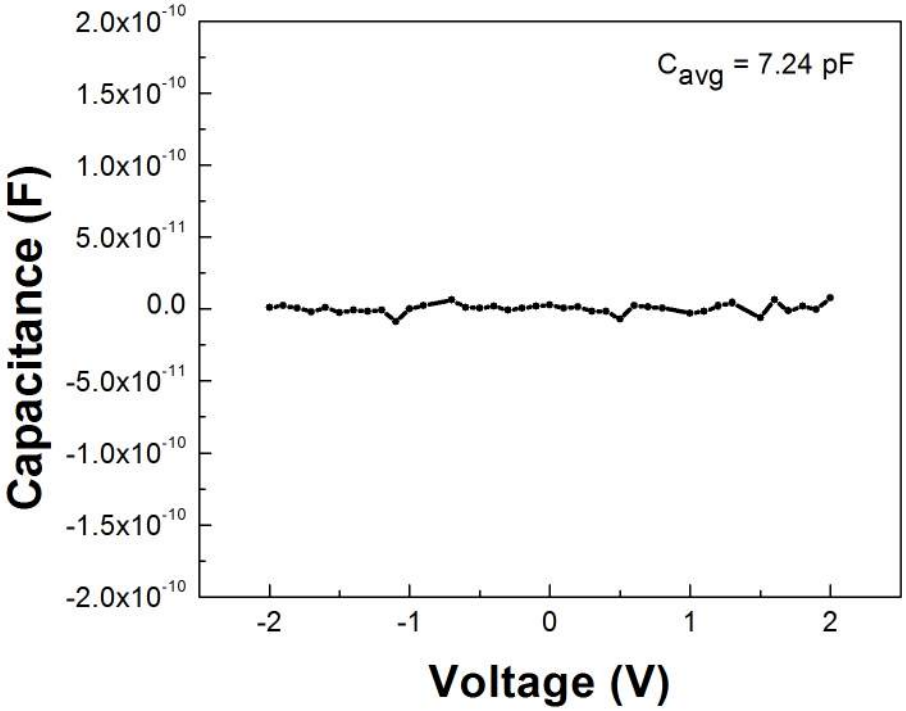

Figure 4.12: C-V Plot for 20 nm HfO_2 based MIM

less flat compared to copper but more with respect to aluminum. Also, the current is relatively high for low thickness and vice-versa.

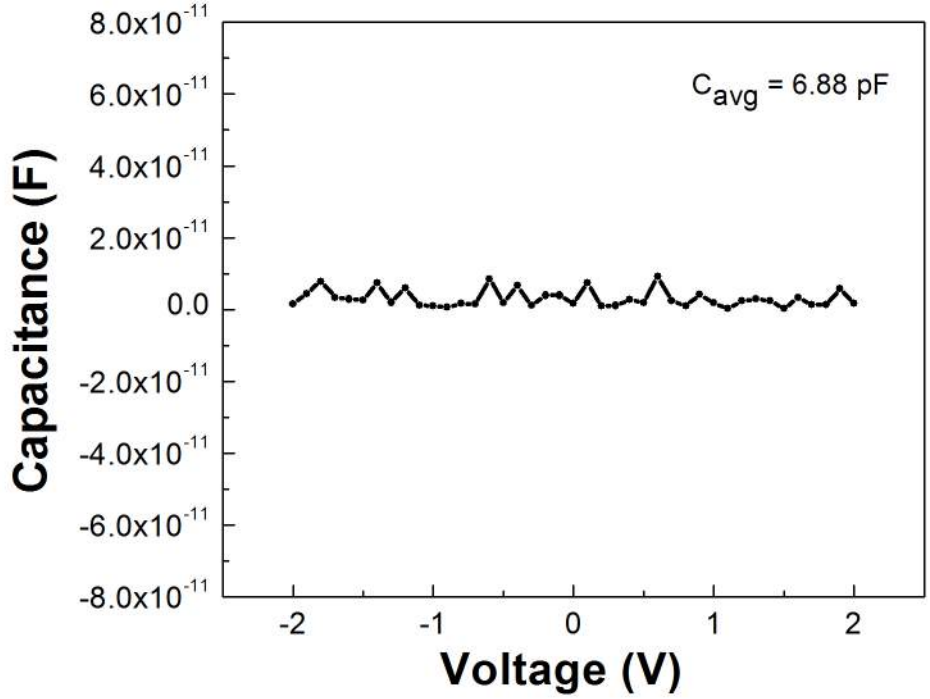

Figure 4.13: C-V Plot for 30 nm HfO_2 based MIM

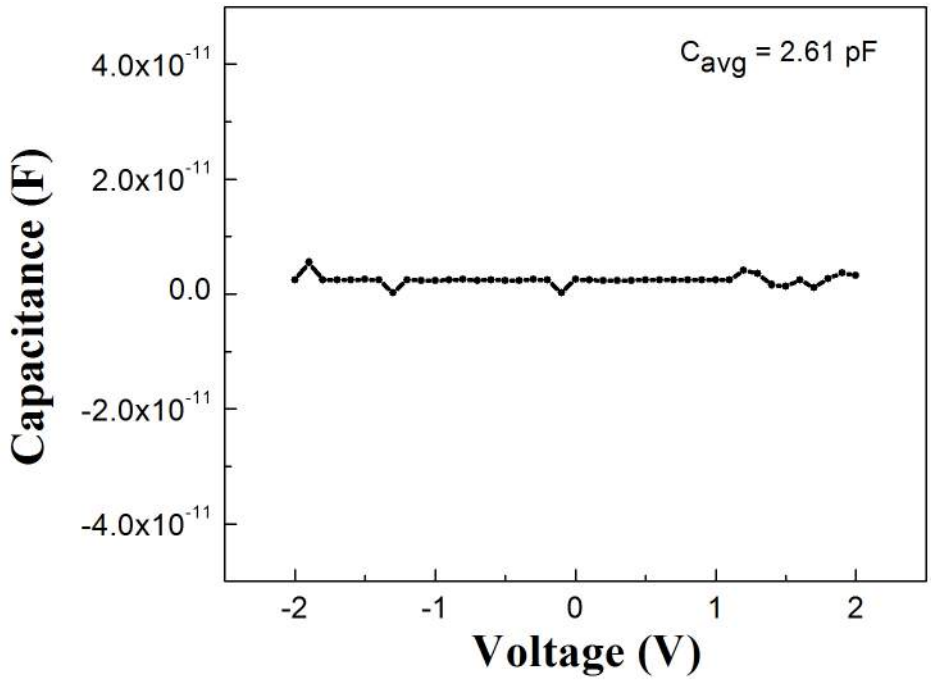

Figure 4.14: C-V Plot for 40 nm HfO_2 based MIM

The following two graphs represent the output characteristics and leakage current associated with the 20 nm thick HfO_2 dielectric TFT.

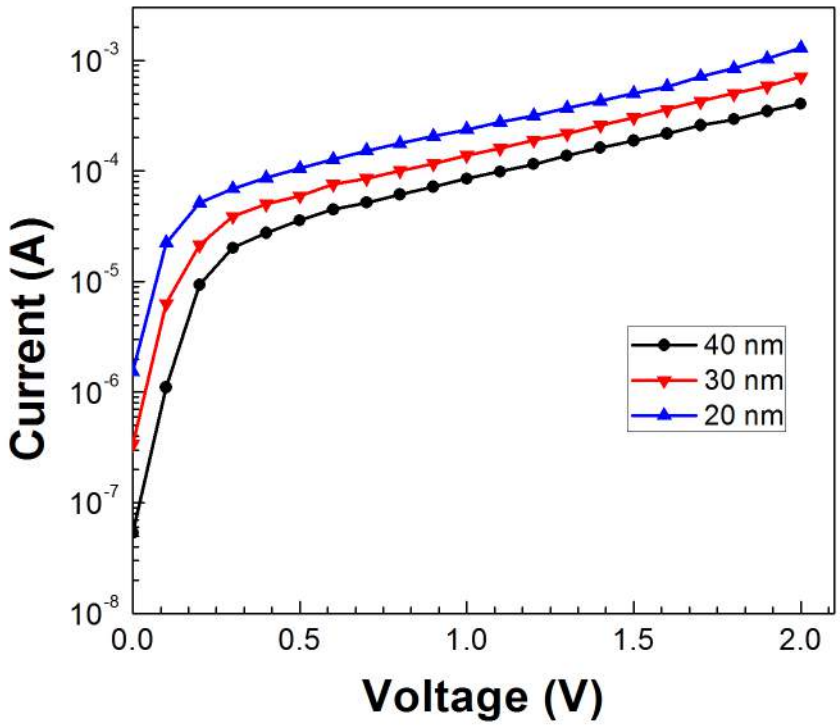

Figure 4.15: I-V of MIM structure with Al as gate for different dielectric thickness

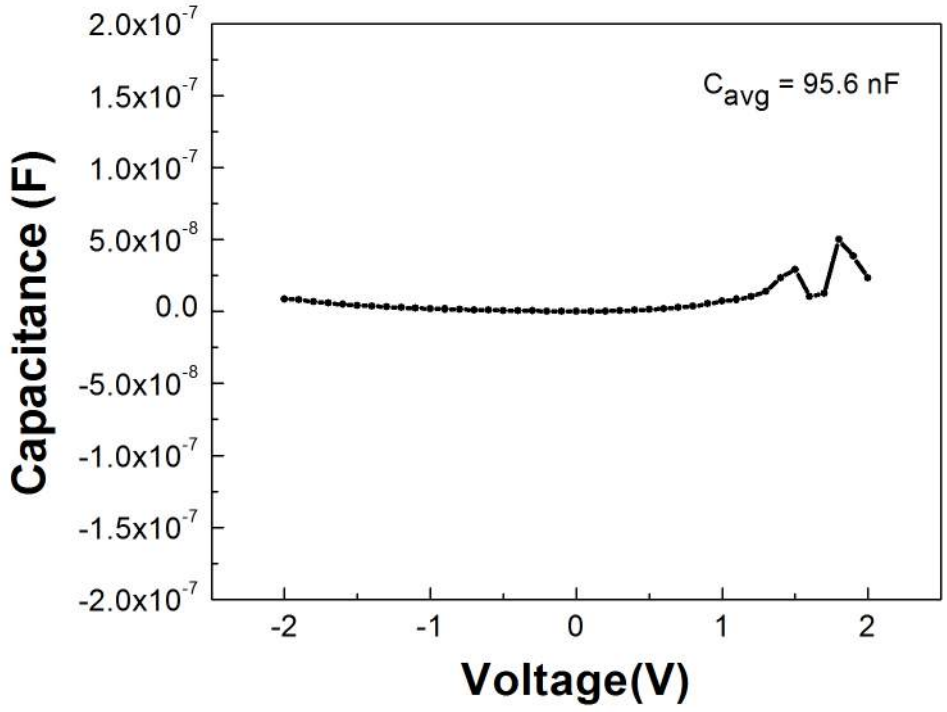

Figure 4.16: C-V Plot for 20 nm HfO_2 based FET

This FET has a very slow linear region with around 0.15 mA as drain current for a gate voltage of 1V and also saturates at relatively higher voltages. The leakage is quite low up to a gate voltage of 0.5 volt but suddenly increases after that and might contribute to the current between source and drain.

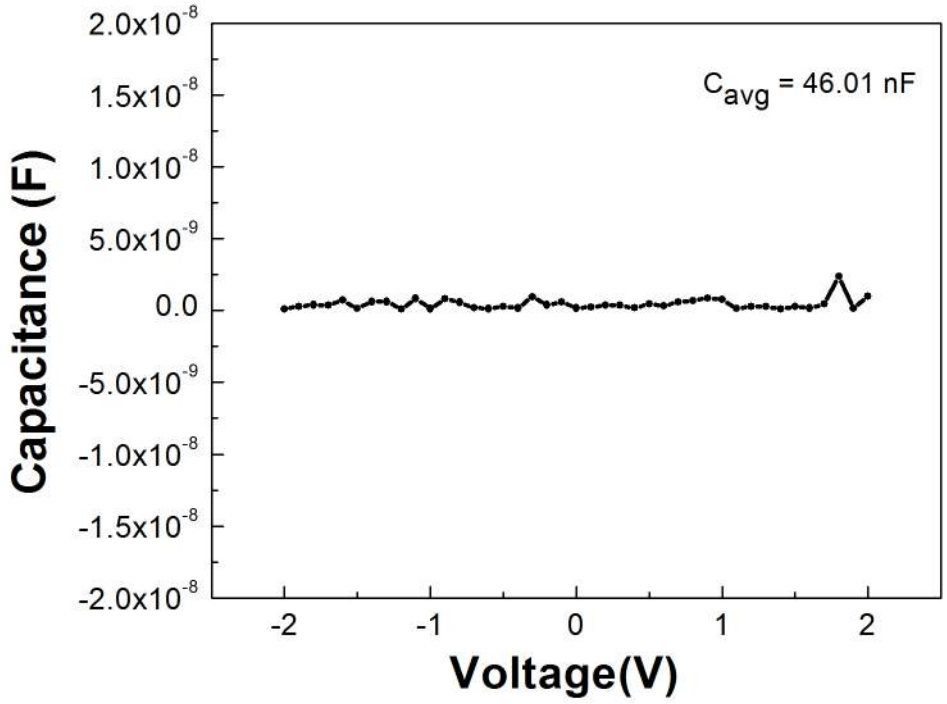

Figure 4.17: C-V Plot for 30 nm HfO_2 based FET

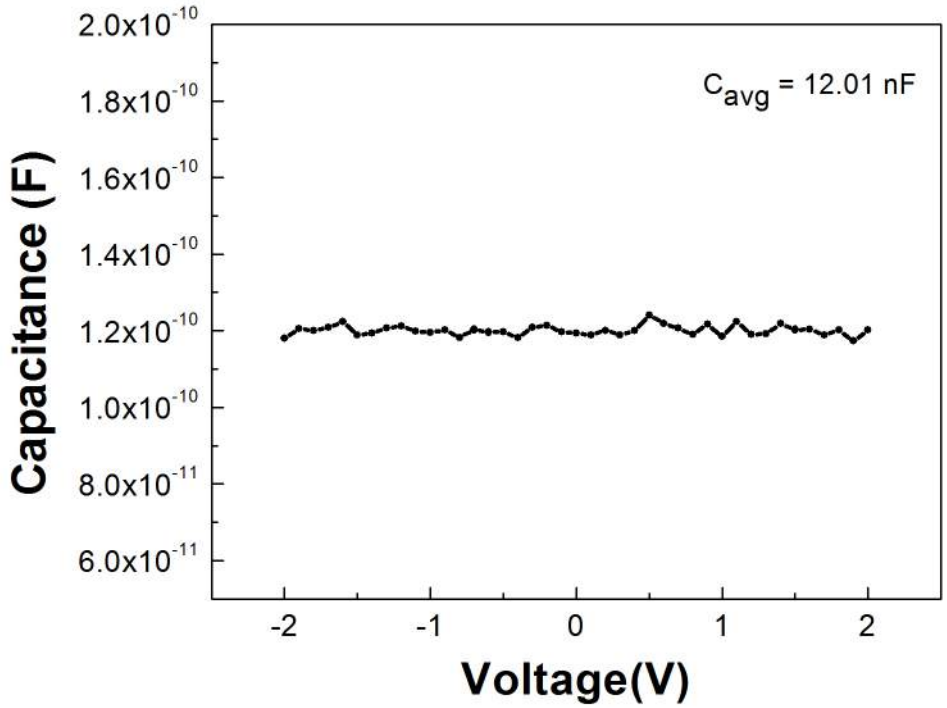

Figure 4.18: C-V Plot for 40 nm HfO_2 based FET

The following two graphs represent the output characteristics and leakage current associated with the 30 nm thick HfO_2 dielectric TFT.

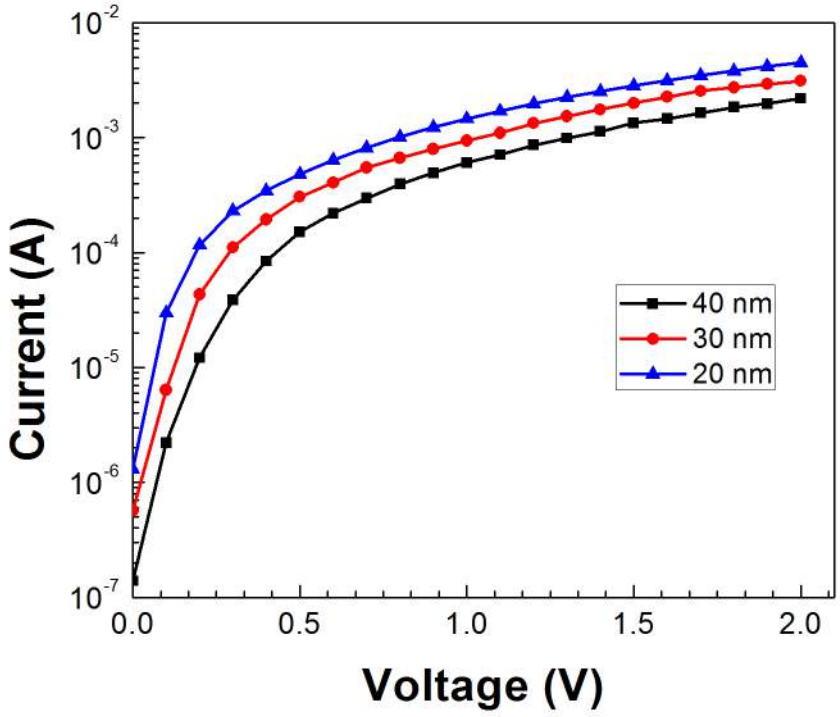

Figure 4.19: I-V of MIM structure with p^{++} as gate for different dielectric thickness

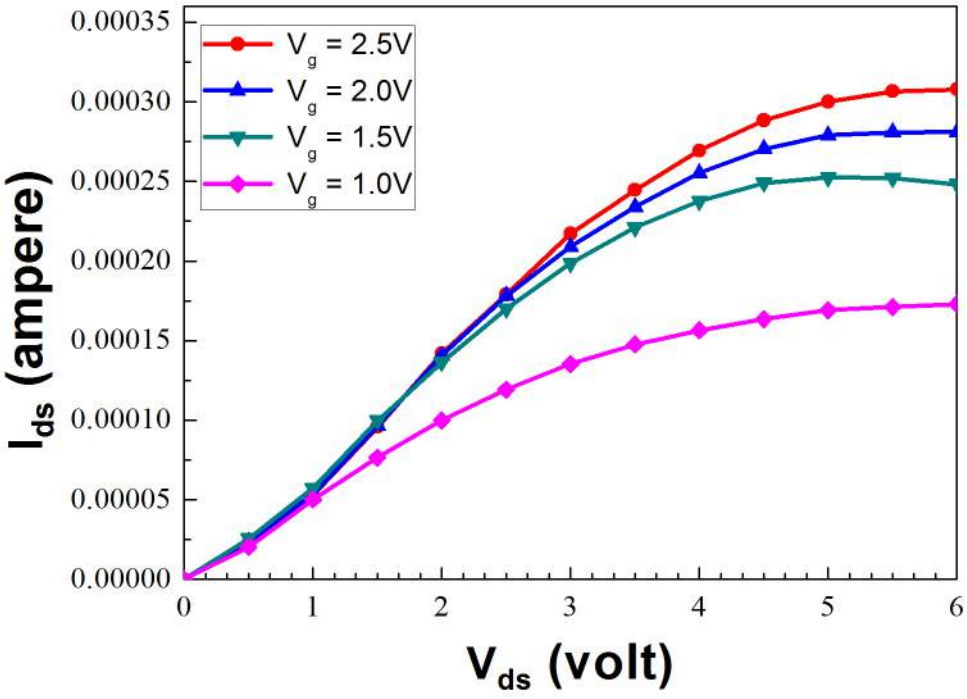

Figure 4.20: Output of FET structure with 20 nm thick dielectric and p^{++} silicon as gate

This has a relatively moderate linear region as well as saturation. The magnitude of channel current is almost similar compared to the previous FET but the leakage is quite low due to increase in

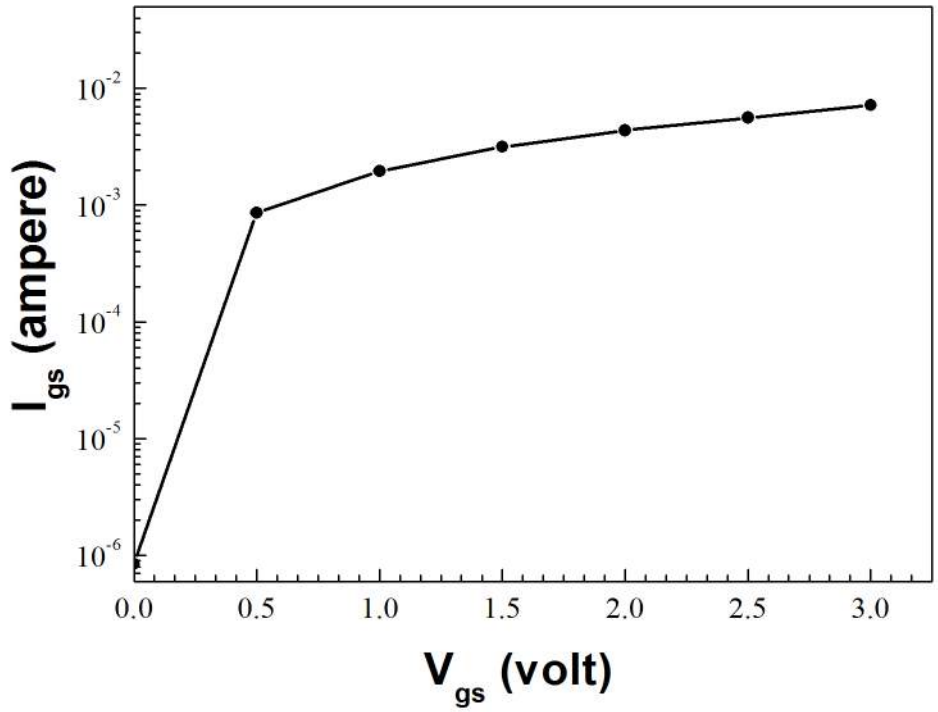

Figure 4.21: Leakage of FET structure with 20 nm thick dielectric and p^{++} silicon as gate

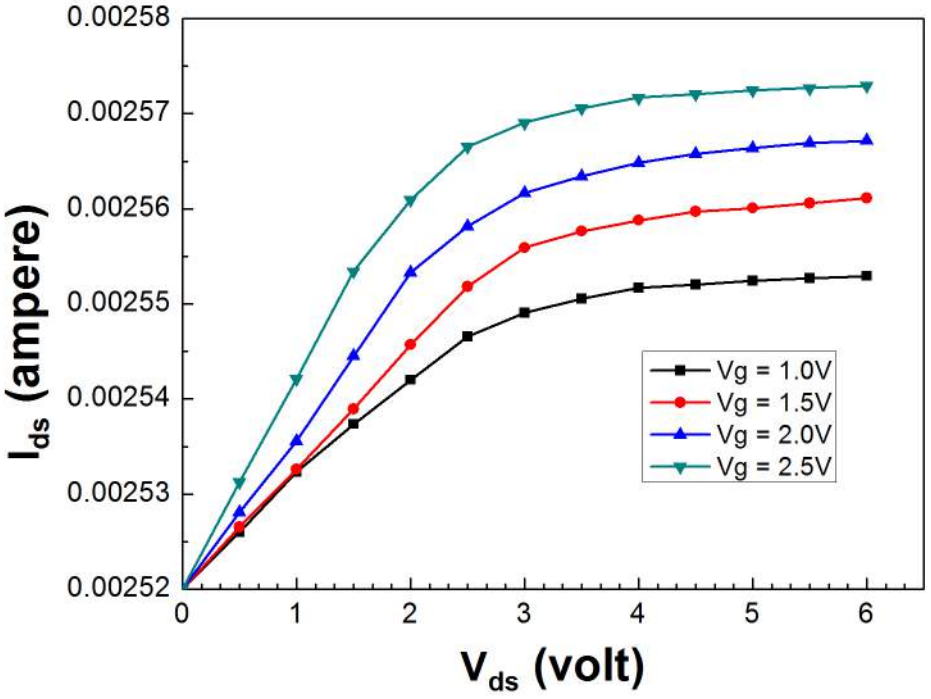

Figure 4.22: Output of FET structure with 30 nm thick dielectric and p^{++} silicon as gate

dielectric thickness. The leakage is significantly low even at 2 or 3 volts and has almost no contribution to the drain current. This condition is optimum for the working of an n-MOSFET at gate voltage of 0-3 V.

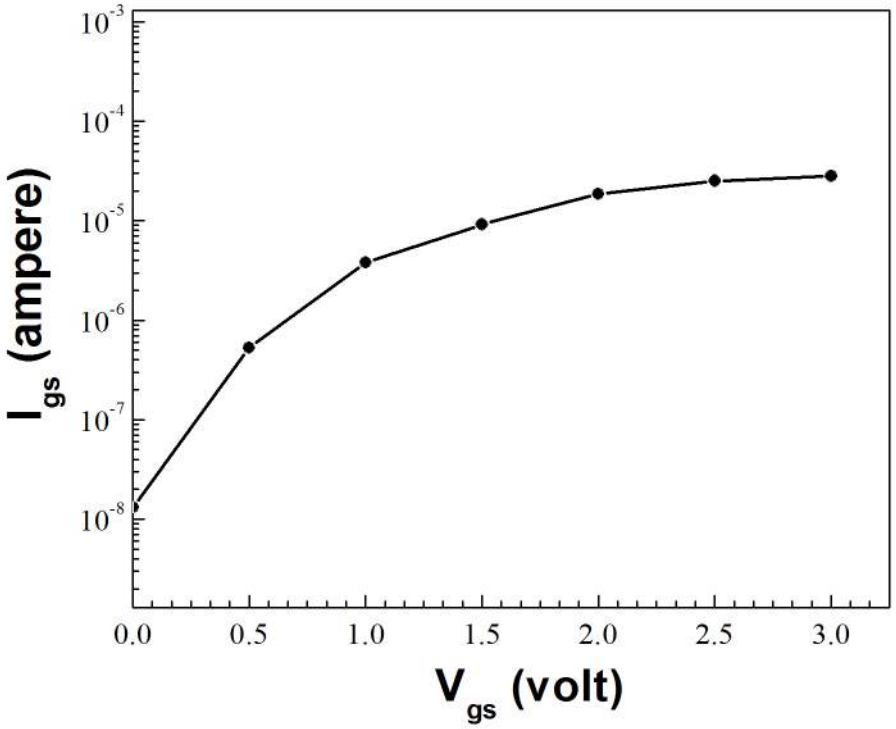

Figure 4.23: Leakage of FET structure with 30 nm thick dielectric and p^{++} silicon as gate

The following two graphs represent the output characteristics and leakage current associated with the 40 nm thick HfO_2 dielectric TFT.

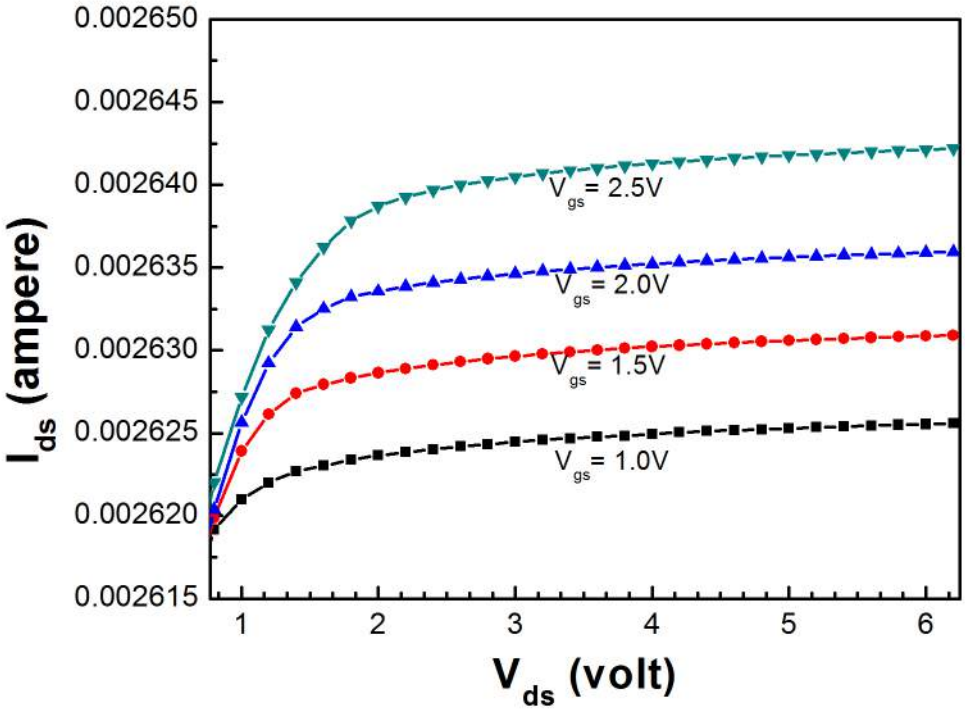

Figure 4.24: Output of FET structure with 40 nm thick dielectric and p^{++} silicon as gate

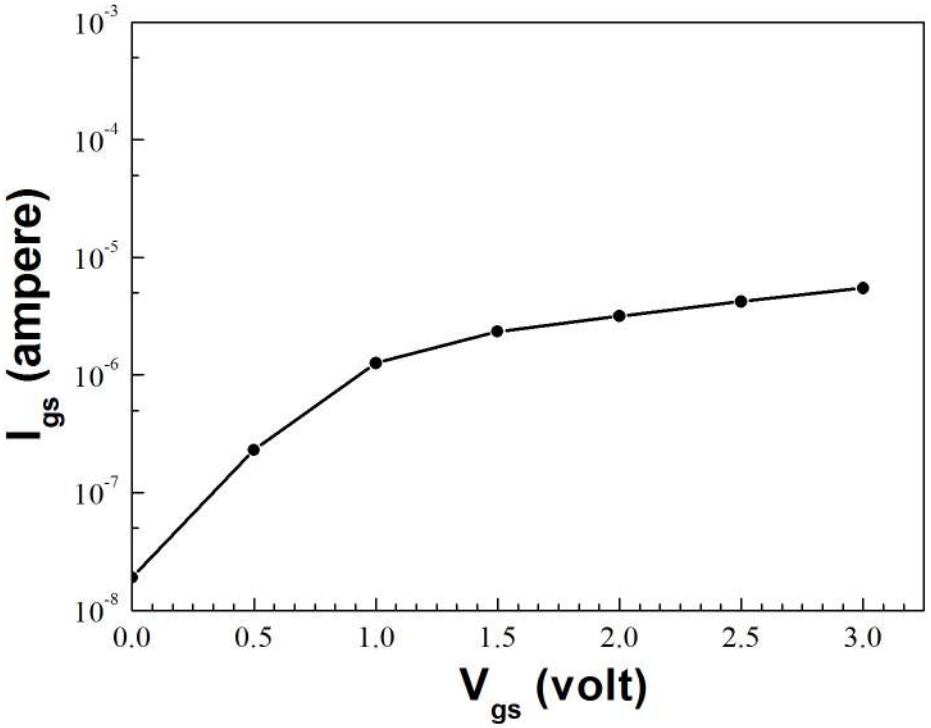

Figure 4.25: Leakage of FET structure with 40 nm thick dielectric and p^{++} silicon as gate

This FET has very fast linear region because of the high carrier mobility in ZnO besides the fact of channel length being very short. It almost gets saturated in around 1 to 2 volts for various gate voltages. This TFT has even much lower leakage (often ideal) compared to 30nm FET which is quite obvious as the physical thickness of dielectric layer has increased but the capacitance density has decreased.

The following graph gives information about the comparison of leakages with variation in thickness of dielectric layer in FET.

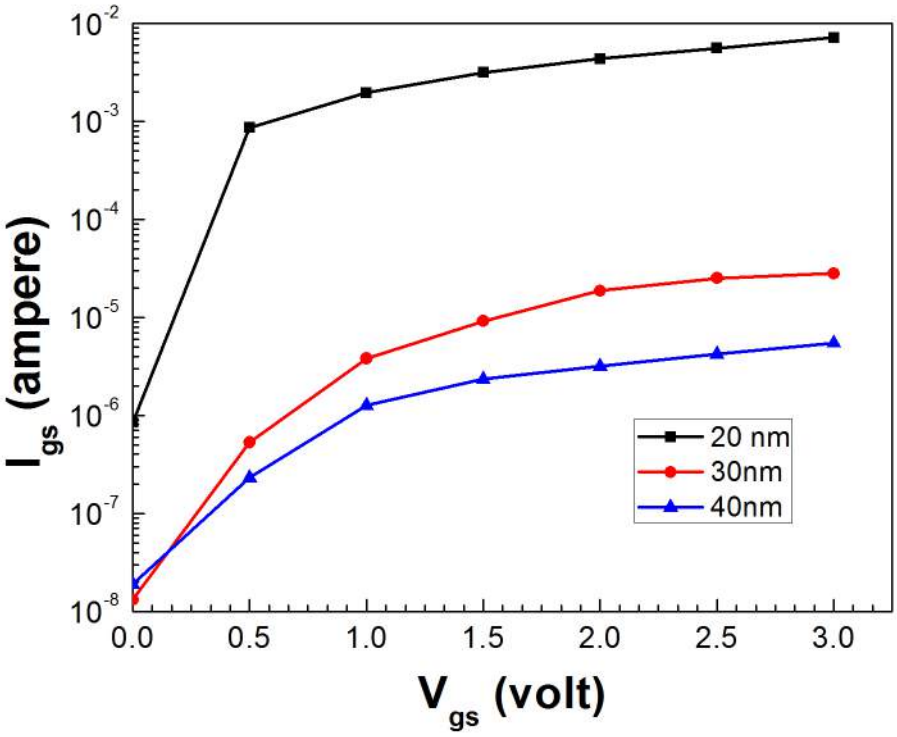

Figure 4.26: Leakage comparison of all TFTs with different dielectric thickness

Chapter 5

Summary and Future Scope

It can be summarized that the copper and aluminum gate materials showed sufficiently more leakage compared to p^{++} silicon substrate as seen from I-V curves of their MIM structures and hence were not ideal for FET fabrication. The copper substrates lacked proper flatness & smoothness and hence deposition of sputtered atoms were not uniform thereby degrading the quality of oxide dielectric film. Using aluminum gate material showed low leakage but very low capacitance density, while on the other hand, those structures on copper substrate showed relatively higher capacitance density but also had high enough leakage compared to aluminum. The structures with p^{++} silicon showed the highest capacitance density among all three and also low leakage compared to copper but similar or little higher than aluminum. Hence, hafnium oxide proves to have better compatibility and good thermal stability with silicon wafer as stated. The 30 nm FET offered ideal output characteristics showing signs of faster switching and good response for coming back to off state even if its little late at switching on. The 20 nm FET has good output curve but experiences enough leakage. The 40 nm FET saturates very fast and has very low leakage but has lower capacitance density. Hence, the 30 nm and 40 nm FET stand out good on a trade-off between both the electric field or channel conduction and gate oxide tunneling leakage. These two FETs have leakage trend much far away from the 20 nm FET. So, 30 nm TFT can function better than 20 nm TFT when it comes to leakage but 20 nm can be applicable where one requires a slow and late saturation at higher source-drain voltages.

As discussed about the properties of ZnO, this transistor can be studied for channel current versus time response and other sensor characteristics while acting as a UV photodetector, gas sensor and many other applications due to the versatility of the zinc oxide semiconducting layer to react differently with different sources in ambient. The TFT fabricated can be characterized by changing the crystallinity of the zinc oxide layer by annealing or giving different substrate temperatures while sputtering the layer. This will change the carrier mobility, channel conduction, change defect concentration within the channel and offer changes with the amorphous oxide interface. Research can also be carried out by doping either ZnO or HfO_2 or both. One can use indium tin oxide (ITO) layer over glass substrate and use it as gate material for the hafnium oxide, zinc oxide combination of TFTs or someone can try coating a conducting gate layer on a flexible substrate and then use this combination to prepare FET. One may investigate the properties using stack layers of SiO_2 or other high-k dielectrics along with HfO_2. Because of several properties associated with the oxide-semiconductor, metal-semiconductor and metal-dielectric interfaces, it becomes quite difficult to optimize all the properties. If we gain one property, we have to compensate or lose the other advantage. So, it is upon investigation that we decide which property we need the most and then optimize it keeping in focus that the sample/substrate/system is not damaged. Because of high range of choice in high-k dielectrics, it remains a long quest to identify the best for a particular purpose and then utilize it on chips to follow Moores law or use in some other applications.

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